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Application Note 110

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NS3D02 APLL Calculation and Simulation Tool – User Instruction Manual, Version 1.0 Download

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For: NS3D02 APLL Loop Filter Simulation and Optimization

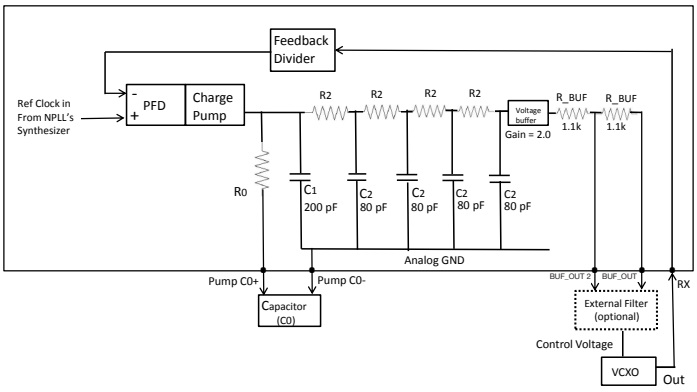
Tool Purpose: Calculate loop dynamics, phase margin, and bandwidth for external VCXO configurations

Loop Filter Configuration Summary

APLL Configuration

The analog PLL (APLL)'s function in NS3D02 is to discipline the external VCXO to output up to two divided down clocks. The APLL will take a clock synthesized by the NPLL as its reference input, translate the frequency to higher frequency and also attenuate the jitter generated by NPLL's digital clock synthesizer.

NS3D02's APLL circuit contains a phase frequency detector (PFD), a programmable charge pump, an uncompleted programmable passive low-pass filter (LPF), a fixed-gain voltage buffer, and a programmable clock feedback divider. With some extra external capacitors to complete the LPF, the APLL can operate to cover loop bandwidth ranging from 10Hz to 200 Hz easily.



The APLL simulation tool models the NS3D02's analog loop filter as a 2nd-order passive loop. Unlike traditional PLLs where the full loop filter is external, the NS3D02 requires only a single external capacitor (C0).

The internal loop filter includes:

- R0 (internal, programmable) – configures integrator resistance.
- R2 (internal, programmable) – configures loop zero location.
- C1 and C2 (internal, fixed) – set the dominant poles in conjunction with R0/R2.

These parameters are configured through NS3D02 register fields:

- APLL_R0_VALUE_L/S R0 setting
- APLL_R2_DIV R2 divider
- APLL_CP_CURRENT Charge pump current (sets loop gain)

External Input:

- C0 is the only value that must be supplied to complete the filter.
- Suggested range: 10 nF to 220 nF, C0G/NP0 ceramic type.

Designers must also input the VCXO tuning gain (Kv, in ppm/V), which heavily influences loop dynamics. A range from 10–100 ppm/V is typical.

1. Calculation Tool Overview

This tool simulates the APLL (Analog Phase-Locked Loop) within the NS3D02 chip by modeling the APLL's internal filter topology completed by a single external capacitor (C0), charge pump, and VCXO. It calculates the resulting loop bandwidth, damping, and phase margin to assist in optimizing jitter performance and lock stability.

The user defines input parameters through hotkey-driven selections, and the tool outputs key loop characteristics and stability metrics.

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9CO NF1011/rev4
  Simple Calculation Tool (09/2023), by  Dr. Andrew Chang
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SETTING:
  [K] KVCO        = +1.00000  ppm/V ..... VCXO's gain
  [0] C0          = +1.00000 uF ......... LPF CAP @ pin(PUMP_C)
  [1] C_ext1      = +1.00000 nF ......... LPF CAP @ pin(BUFOUT2)
  [2] C_ext2      = +1.00000 nF ......... LPF CAP @ pin(BUFOUT) & VCXO's CV
  [F] freq(PFD)   = +1.00000 kHz
  [R] R0          = (1=SM) idx(   1) .... see REG table
  [B] BW2's R2s   =        idx(   1) .... see REG table
  [I] CP current  =        idx(   1) .... see REG table

CALCULATION/SIMULATION RESULTS:

       freq(-3dB) ................ = +6.17 mHz
       1st-order motion ......... = (zeta=0.000) (tau=+780. ksec)
       Phase Margin ............. = +0.2 deg

       <ps> Some information won't be listed
            Simulation was aborted due to inappropriate setting

HOTKEY: Change Setting: ............. [K012FRBI]
       Show Xfer Funtions H, He ... [H]
       Quit/Exit: .................. [Q] .............. ?
```

2. Interface Layout

Hotkeys for Parameter Input:

Hotkey	Parameter	Description
[K]	KVCO	VCXO tuning gain (ppm/V) – converted to Hz/V internally
[0]	C0	Capacitor at charge pump (µF)
[1]	C_ext1	Optional cap at BUF_OUT2 (nF)
[2]	C_ext2	Optional cap at BUF_OUT (nF)
[F]	PFD Frequency	Phase Frequency Detector frequency (kHz)
[R]	R0	Main LPF resistor index
[B]	R2	Secondary LPF resistor index
[I]	CP Current	Charge pump current index

Command Hotkeys:

Hotkey	Function
[H]	Show loop transfer functions
[Q]	Quit the simulation tool

3. Input Instructions

Start the tool and observe the current parameter values.

Press a hotkey to change a setting. For example:

- Press K, then enter 80 sets VCXO gain to 80 ppm/V
- Press F, then enter 100 sets PFD to 100 kHz

Adjust all components to realistic values based on your VCXO and target loop behavior.

The tool automatically updates the simulation output after each parameter is changed.

4. Simulation Outputs

Displayed Results:

- freq(-3dB): Approximate loop bandwidth (Hz)
- 1st-order motion: Loop damping and time constant
- Phase Margin: Stability metric (target 45–65°)

If simulation is aborted, revise any extreme or unrealistic values (e.g., too large C0 or too low CP current).

5. Troubleshooting Common Errors

Symptom | Likely Cause | Suggested Fix

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Phase Margin < 5° or > 90° | Loop gain or component mismatch Adjust C0, R0, or CP current

freq(-3dB) < 1 Hz | Oversized C0 or weak KVCO | Reduce C0, increase CP current

Simulation aborted | Invalid configuration | Rebalance PFD frequency, loop filter values

VCXO doesn't lock | Control voltage range mismatch | Ensure VCXO tuning range is correct

6. Design Guidelines

Target Phase Margin: 50–65°

Typical Loop Bandwidths: 10–200 Hz

VCXO Gain (KVCO): 10–100 ppm/V typical

Charge Pump Currents: 10–200 µA

PFD Frequencies: 8 kHz to 1 MHz

7. Reference Registers (NS3D02)

APLL_CP_CURRENT – Sets charge pump current

APLL_REF_FREQ – Sets reference input frequency

APLL_R0_VALUE_L/S – Sets main filter resistor (R0)

APLL_R2_DIV – Sets secondary resistors (R2)

8. Saving/Sharing Designs (Optional Feature)

If your tool supports configuration export:

- Press S to save current settings
- Use .apllcfg or .json format for structured configuration
- Include metadata such as timestamp and notes

9. Exit the Tool

To exit, press [Q]. You will be prompted to confirm quitting.

10. Support and Feedback

For help with this tool or NS3D02 designs:

- Website: www.conwin.com
- Email: support@conwin.com
- Reference Document: TM144 – NS3D02 Datasheet

Download Calculation tool HERE: