EH321-TFC-CC-series 1PPS Time to Frequency Conversion OCXO Module

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DATA SHEET

RoHS COMPLIANT

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Overview

The EH321 Series OCXO module is a highly integrated time and frequency synchronizing solution. The design implementation is intended to support high precision clock generation where precise accuracy, high frequency stability and time synchronization is required. This OCXO module can operate with or without a 1PPS incoming signal. When a 1PPS signal is present, the module will automatically phase and frequency lock to the 1PPS input reference at a user defined loop bandwidth setting and generate a clock output phase aligned to the rising edge of a synthesized 1PPS output. The clock output frequency is based upon the frequency an internal, low-noise VCXO, which establishes the characteristics of the clock output signal. The internal VCXO can be configured with a frequency from 10MHz to 156.25MHz.

When the 1PPS incoming signal is lost, the module enters into holdover mode at its last held position in phase and frequency. The on-board OCXO provides the stability of the holdover period until a valid 1PPS signal returns. When provisioned with a Temp sense enabled (TSE) OCXO module, the internal logic can automatically compensate for frequency offsets generated inside the OCXO to enhance the stability of the OCXO in operation and during holdover or free run periods.

This product can be used to support applications requiring recurring and precise calibration, extremely high frequency stability and where a time stamp reference is required with low jitter clocking. Internal registers are accessible through I2C communication for system programming and monitoring.

Features

- Accepts 1 PPS Reference input
- Phase and Frequency locked outputs
- LOS, LOCK and Holdover indication
- Low Noise Clock output (10MHz typical)
- Flexible frequency output options available
- 1PPS Auto-detect
- Automatic entry into holdover
- 3.3VDC Supply Voltage
- Phase and Frequency locked outputs
- -40°C to 85°C operating temperature range
- OEM SM footprint 25 x 22 mm
- RoHS Compliant

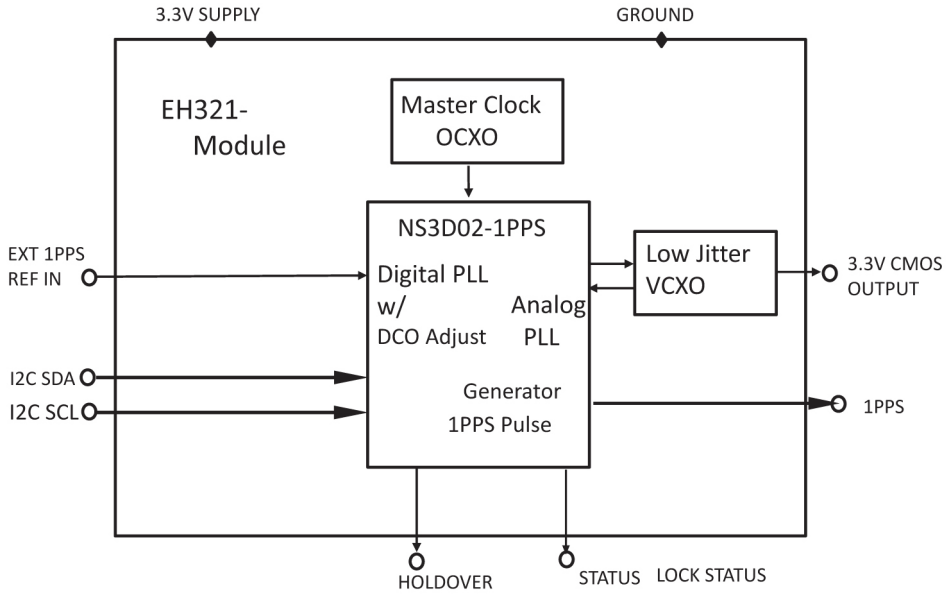

Figure 1: EH321 Functional Block Diagram

General Description

The EH321 is a fully integrated numerical PLL based time and frequency synchronizing module that receives a single 1PPS reference input and generates a 1PPS output and a single ended clock output phase locked and aligned to the rising edge of the 1PPS output pulse.

The design architecture incorporates a sophisticated digital and analog PLL scheme to provide a low jitter phase/frequency locked clock output at a single frequency in the range from 1MHz to 156.25 MHz as well as a 1PPS pulse output. The system is clocked with an internal precision OCXO providing the basis for holdover and free run performance when a 1PPS reference input is not present. The EH321's NPLL (Numerical PLL) can be programmed for filter bandwidths from 100mHz to less than 1mHz for disciplining the incoming 1PPS signal

The module digitally synthesizes two outputs from the timing generator, one clock and a 1PPS pulse output. The 1 PPS pulse is brought out directly from the NPLL synthesizer and the clock output functions as reference input to the module's follow on APLL (Analog PLL) circuit within the module. The analog portion of the module consists of an independent APLL circuit with integrated charge pump and phase detector, supported by an internal VCXO, that translates the frequency and attenuates the jitter on the synthesized clock output generated in the NPLL section of the module. An LVCMOS single ended output clock is derived from a disciplined VCXO. The internal VCXO provides the output characteristics for phase noise and jitter performance for the clock output from the EH321. The clock output transmitter has a 6-bit follow on divider circuit available for dividing the frequency of the VCXO. VCXO frequencies can be chosen between 10MHz and 156.25MHz.

The EH321 module has functionality for automatically calibrating its internal master clock (MCLK) when using a temperature sense enabled (TSE) OCXO module. This allows for a compensation scheme to support stability enhancement and high precision holdover performance of 1.5 uS over 8 hours.

Internal NPLL, a Numeric Timing Generator

The kernel of the EH321 is a NPLL (Numerical-based PLL). In its core, all internal modules are either digital or numerical, including the phase detectors, filters, timing generator and clock synthesizers. The pure digital design timing generator allows the EH321 to become an accurate and reliable deterministic system. Connor-Winfield's synchronization ASIC NS3D02 is the timing engine in the EH321 module. Through the I2C communication pins, the registers in the NS3D02 that are factory programmed and set in a pre-determined default mode, can be adjusted by the user to change certain "run-time" functions and settings, as well as monitor system performance through a set of "read-only" registers.

For example, the user can an internal phase adjustment register to correct for sawtooth error jitter in an externally controlled GNSS receiver when quantization error messaging is provided by the receiver. Estimates of where the next 1PPS pulse will fall can be used to reduce the jitter caused by this saw tooth error. A full description of the NS3D02 functionality and registers can be found in the NS3D02 data sheet.

For more detailed information on the operation of the internal system ASIC NS3D02, see the following data sheet. http:// www.conwin.com/datasheets/tm/tm144.pdf

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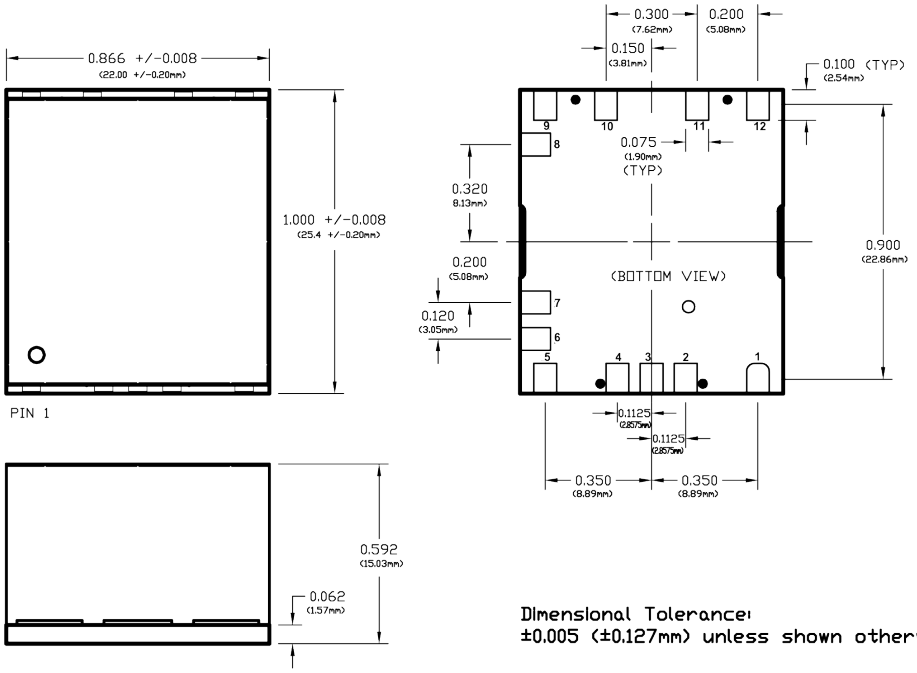
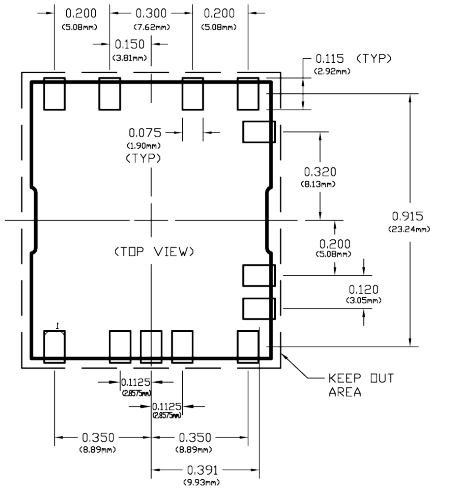
2 Physical Characteristics

The EH321 is a multi-chip module (MCM) built on an FR4 fiberglass 22x25mm PCB.

Mechanical Drawing



Suggested Pad Layout



KEEP OUT AREA
UNDER THE PCBOARD IS A KEEP OUT AREA,
DO NOT PLACE ANY PARTS IN THIS AREA.

Figure 2 EH321-TFC-CC Mechanical Drawing and Suggested Pad Layout

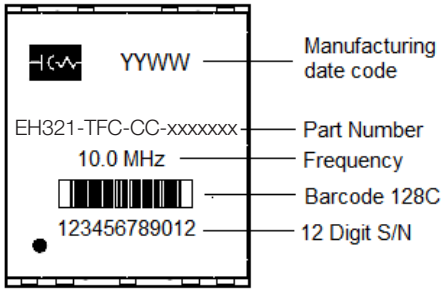


Figure 3 Marking Configuration

Pin	Function	Notes
1	1PPS_IN	
2	GND Analog	
3	1PPS_OUT	
4	GND Analog	
5	VCC_3V3_Digital	
6	LOCKED	
7	HOLDOVER	
8	GND_Digital	
9	FREQ_OUT	
10	I2C SCL	
11	12C SDA	
12	GND_Digital	

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3 Signal Descriptions

The signals on the EH321 are described in the table below.

3.1 Power Signals

VCC_3V3	Type:	Power Direction: Input	Pin: 5
	The Supply Input. This 3.3V ± 10% input supplies power to the module		
GND	Type:	Power Direction: Input/Output	Pin: 8 and 12
	The Input Ground. This is the return path for the vcc 3V3 supply and the ground for the module.		
GND ANALOG	Type:	Power Direction: Input/Output	Pin: 2 and 4
These are analog grounds for output pin 9.			

3.2 I/O Signals

TX[0]	Type: I/O	Direction: Output	Pin: 10
	I2c SCL PIN		
RX[0]	Type: I/O	Direction: Input	Pin: 11
	I2c SDA PIN		
HOLDOVER	Type: I/O	Direction: Output	Pin: 7
	Standard software builds use this signal to indicate Holdover status. High indicates holdover mode. This signal has a 3.3V CMOS drive.		
LOCKED	Type: I/O	Direction: Output	Pin: 6
	Standard software builds use this signal to indicate LOCK status. High indicates locked to 1pps. This signal has a 3.3V CMOS drive.		
FREQ_OUT	Type: I/O	Direction: Output	Pin: 9
	Primary output of the module which is a pass through of the frequency of the VCXO internal to the module.		
1PPS_IN	Type: I/O	Direction: Input	Pin: 1
	The 1 Pulse-Per-Second Reference Input Signal. This is normally as a 1 pulse aligned with GPS time, generated by an external GPS/GNSS source.		
1 PPS_OUT	Type: I/O	Direction: Output	Pin: 3
	The 1 Pulse-Per-Second Reference Input Signal. This is normally as a 1 pulse aligned with GPS time, generated by an external GPS/GNSS source.		

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4 Operating Specifications

Frequency Stability

Parameter	Minimum	Nominal	Maximum	Units	Condition
Frequency		10.0		MHz	
Initial Frequency accuracy	-1.0	-	+1.0	ppm	@25°C, after 15 mins power on ref to nominal frequency.
Frequency Accuracy	-100	-	+100	ppb	@25°C, Within 90 days after shipment and 5 Minutes warm up time (after reflow), Measurement referenced to initial frequency.
Supply Variation	-1.0	-	+1.0	ppb	Vs±5%,@25°C
Load Variation	-1.0		+1.0	ppb	CL±5%,@25°C
Aging per day	-0.5		+0.5	ppb	
first year	-50		+50	ppb	Aging after 30 days of operation
10 years	-0.5		+0.5	ppm	
Holdover Temperature Stability					-40°C ~ +85°C; (Fmax-Fmin)/2
Code 003	-0.3	-	0.3	ppb	
Code 005	-0.5	-	0.5	ppb	
Code 010	-1.0	-	1.0	ppb	
Short Term Stability (in still air)			0.01	ppb/s	after power on 1hour @25°C
Warm -up time			5.0	min	Within ±10ppb of final frequency with reference after 1 hour on
Start-up Time			1.0	s	

Supply Voltage/Current

Parameter	Minimum	Nominal	Maximum	Units	Condition
Voltage Supply	3.135	3.3	3.465	V	
Supply Current		1000	1200	mA	during warm-up
		250	300	mA	at steady state, 25°C
		550	600	mA	at steady state, -40°C

Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Condition
CMOS Load		15		pF	
Output Level(VOL)			0.4	V	
Output Level(VOH)	3.0			V	
Duty Cycle	45		55	%	
Rise Time/ Fall Time		2.5	4.0	ns	
Spurious			-70	dBc	

Phase Noise

Parameter	Minimum	Nominal	Maximum	Units	Condition
Phase Noise					
@1Hz	-	-90	-		@1Hz
@10Hz	-	-92	-		@10Hz
@100Hz	-	-107	-	dBc/Hz	@100Hz
@1KHz	-	-142	-		@1KHz
@10KHz	-	-160	-		@10KHz

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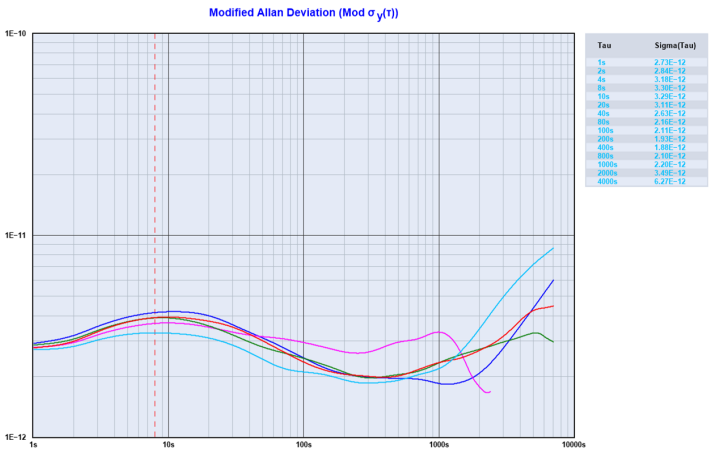
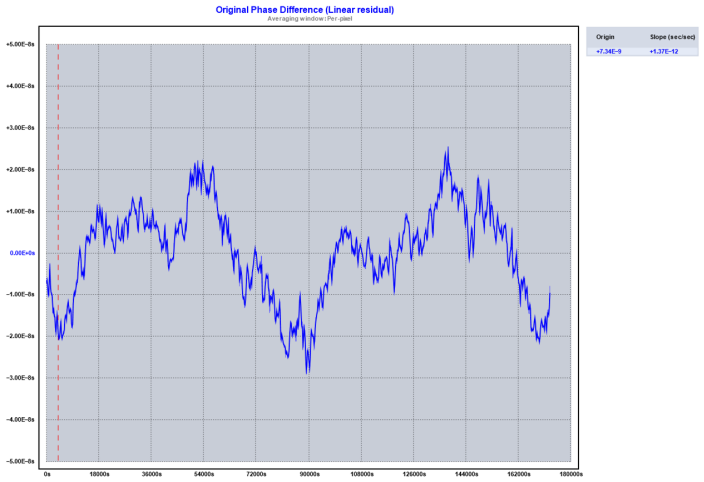
5 Performance Comparisons

The EH321-TFC model series allows for a choice of master clock options which dictate the bandwidth setting chosen to optimize performance. The -CC option allows for loop bandwidth settings of 1 mHz or less due to its master clock ultra-low ADEV performance.

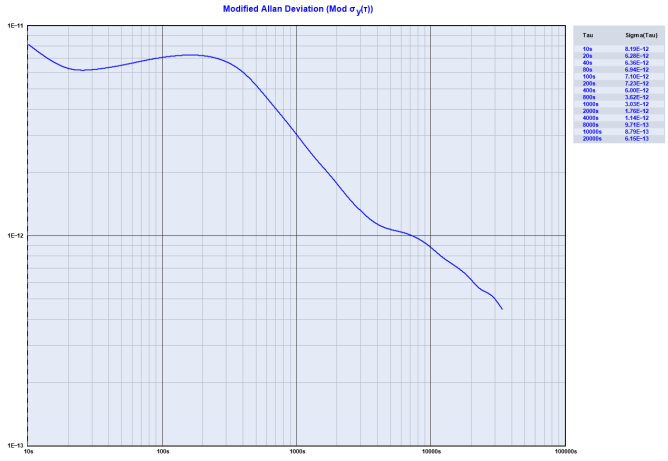
EH321-TFC-CC (in Free run) Modified Allan Deviation Graph



EH321-TFC-CC Phase Tracking (in lock mode)



EH321-TFC-CC (in lock mode) Modified Allan Deviation Graph



EH321-TFC-CC Frequency Difference (in lock mode)

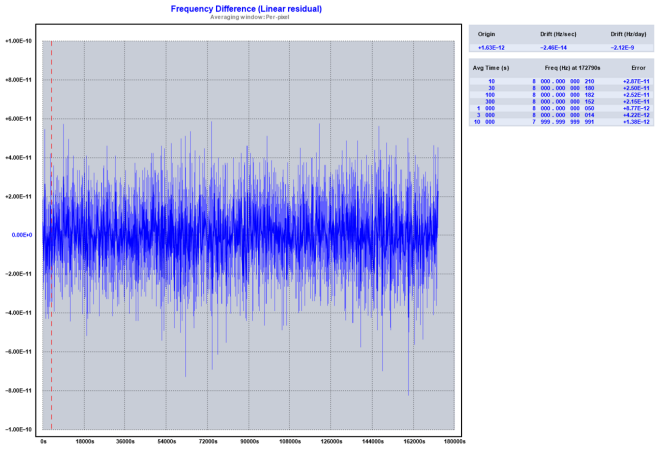


Figure 4: EH321-TFC-CC Performance Comparisons

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6 Tape and Reel Specifications

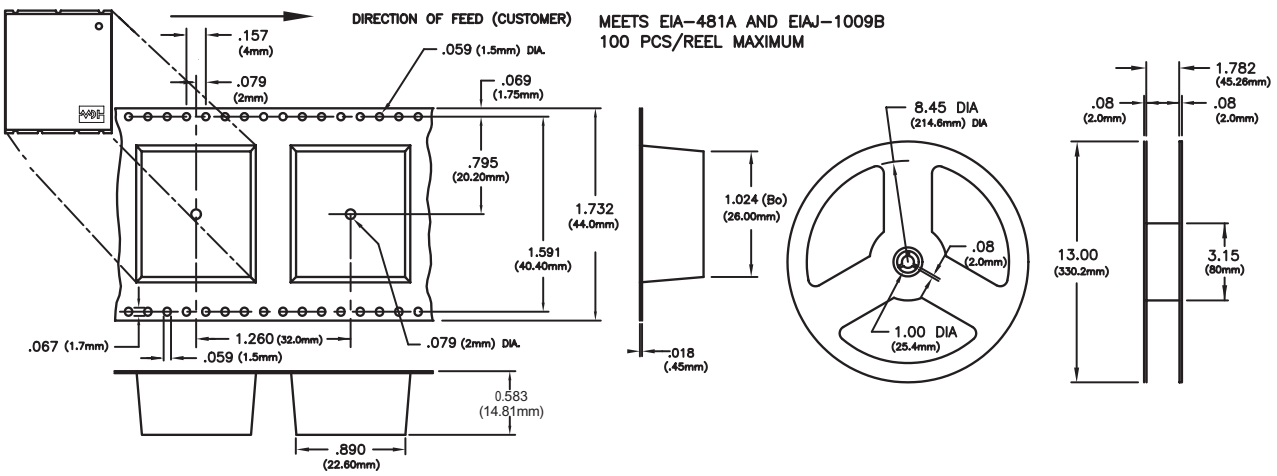

Figure 5 Tape and Reel

7 Solder Profile

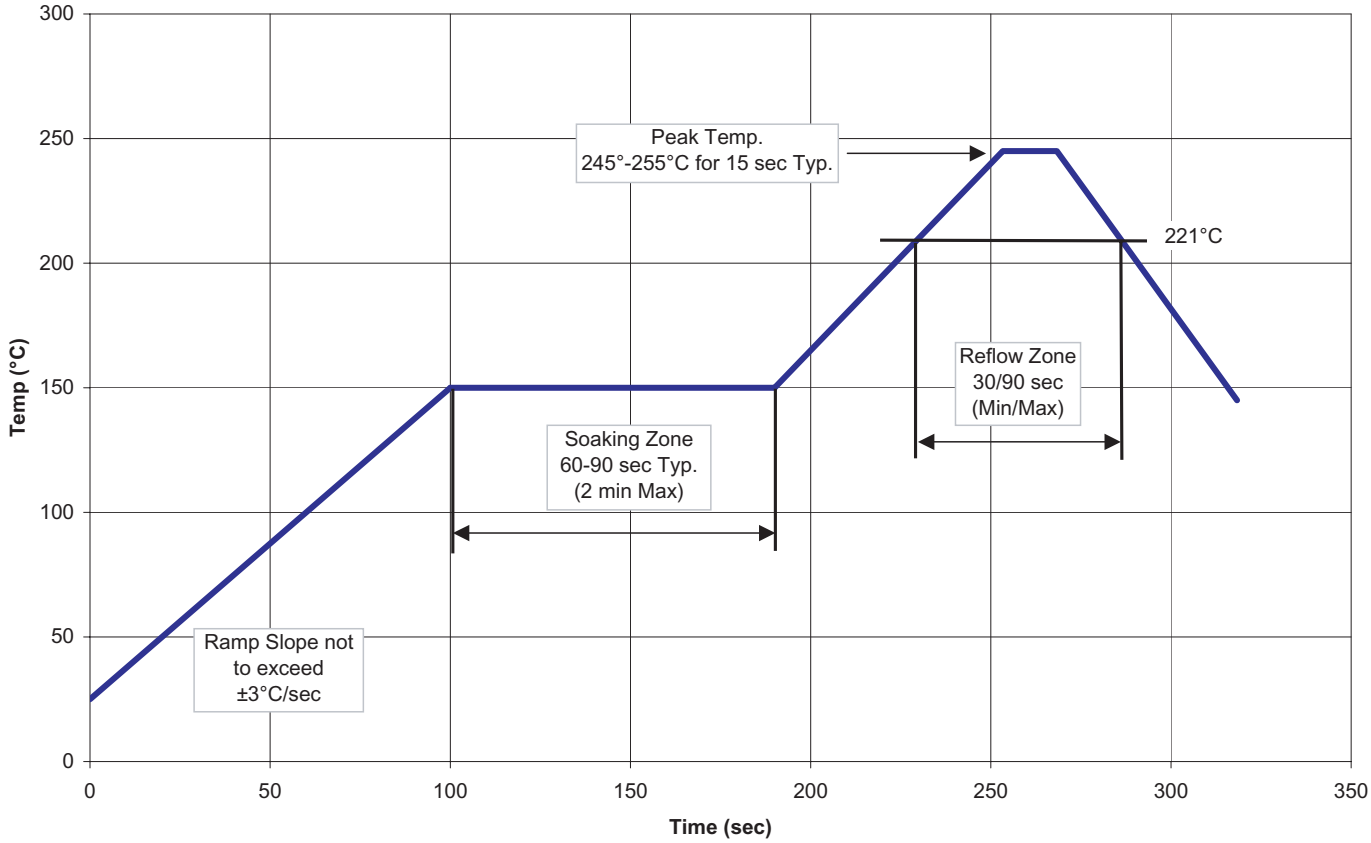

Figure 6 Solder Profile

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EH321-TFC-CC-series
Time to Frequency Converter Module

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Ordering Information

EH321-TFC-CC-	6	003	3	C	F	-010.0M
Type / Package EH321 Part Number Series	Temperature Range: 5 = 0 to 70°C 6 = -40 to 85°C 7 = -20 to 70°C	Frequency Stability 003 = ±0.3ppb 005 = ±0.5ppb 010 = ±1.0ppb	Supply Voltage 3 = 3.3 Vdc	Output Type C = CMOS	OCXO Type F = Fixed Freq.	Output Frequency Frequency Format -xxx.xM Min* -xxx.xxxxxxM Max* *Min of 1 and Max of 6 digits after the decimal point. M=MHz

EH321-TFC-CC-60033CF-010.0M

- BASE MODEL
- Temp Range -40 to 85C
- 3.3V Supply
- Temperature Stability in Holdover ±0.3ppb
- CMOS Fixed Frequency
- Output Frequency

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Revision History

Revision	Date	Note
00	01/04/24	New Release
01	03/21/24	Update package dimensions, pin number table, and add part numbering system table and operating specifications.