Connor Winfield
Delivering a New Generation of Time and Frequency Solutions for a Connected World.

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

D A T A S H E E T

NS2D04-1PPS – GPS/GNSS 1PPS Time to Clock Output Synchronizer

CONNOR WINFIELD

Overview

The NS2D04 -1PPS is a highly integrated time and frequency synchronizing ASIC. This design implementation is dedicated for use in applications which specifically require locking to an incoming 1PPS reference signal. This high precision phase and frequency synchronization solution also integrates low noise frequency generation and/or frequency translation. This product can be used to support a high-stability frequency reference for use in wireless systems, IEEE 1588v2, and applications employing a 1PPS frequency source for high precision, long term time and frequency generation. The NS2D04-1PPS allows the user access to the chip's internal phase detector to calibrate and correct for saw tooth error typically found on a 1PPS signal emanating from a GNSS receiver. Another feature provides the user access to the internal master clock and NCO which can be used to calibrate and correct for drift found in the external supporting OCXO or TCXO. With less than 1 ppt resolution, the user may compensate in holdover mode for frequency instabilities due to temperature change or long term aging characteristics.An external precision OCXO or TCXO provides the system's master clock for various holdover performance options as well as the support for multiple filter bandwidth options from <1mHz to .05 Hz. Up to two external disciplined VCXOs provide the output characteristics for phase noise and jitter performance for any combination of 8 differential or 17 single ended clock outputs with output jitter performance options of sub100fs RMS (12kHz to 20MHz).

Features

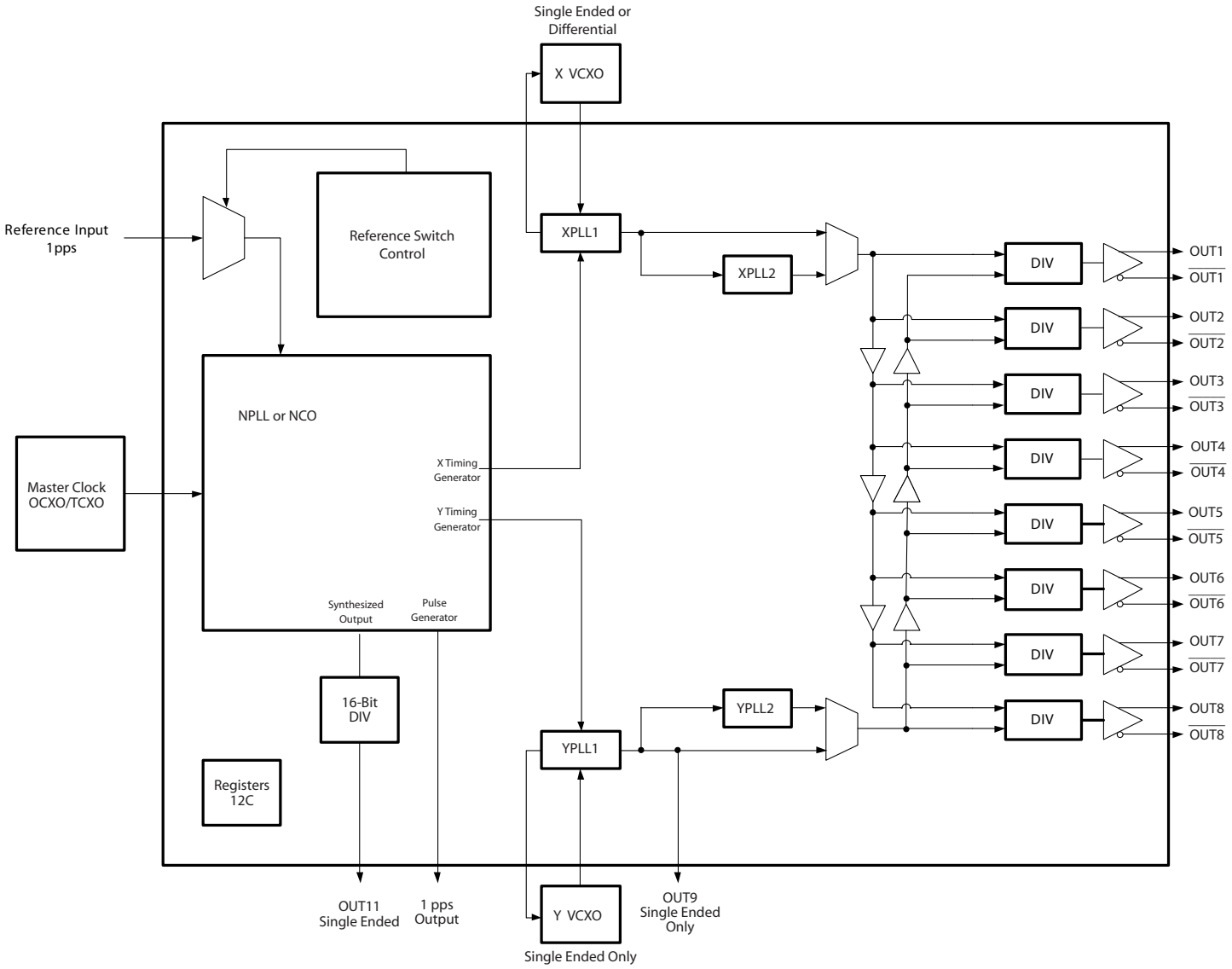
- Accepts 1 PPS Reference input
- Programmable phase alignment of outputs to 1 PPS reference input
- Internal NCO for SAW tooth error smoothing
- Locked, HO, & Free-run indication. Holdover options available to .001ppb resolution
- 1Hz to 800 MHz clock output frequency range
- Eight differential or up to 17 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- Low jitter clock outputs (less than .3ps RMS (12kHz to 20MHz) with options for sub 100fs)
- Programmable bandwidth settings for multiple applications
- I2C Interface for system communication and interrogation.
- 3.3VDC Supply Voltage
- -40°C to 85°C operating temperature range
- 8 x 8 mm 68 pin QFN surface mount package

Applications

- Primary Reference Time Clock (PRTC) [G.8272]
- Telecom Grand Master [G.8273.1]
- Telecom boundary clock [G.8273.2]
- Wireless Base Stations
- GNSS Disciplined Oscillator
- NTP Stratum 0 Standard

Bulletin	TM143
Revision	03
Date	31 Oct 2023

NS2D04-1PPS Functional Block Diagram



NS2D04-1PPS Specifications

Parameter	Specification
Voltage	3.3V ±5%
Power	Based on configuration (300mA with outputs tri-stated) Outputs add: LVPECL 50mA, LVDS 20mA, LVCMOS 8 mA
Temperature	-40 to 85°C Industrial temp range operation
Reference Frequency (1PPS)	1 Pulse Per Second (1Hz) 3.3 V DC ref
Low Jitter Clock Output Frequency	1Hz to 800 MHz
Holdover stability	0.001 ppb capable
Dimensions	8 x 8 x 1mm 68 pin QFN package

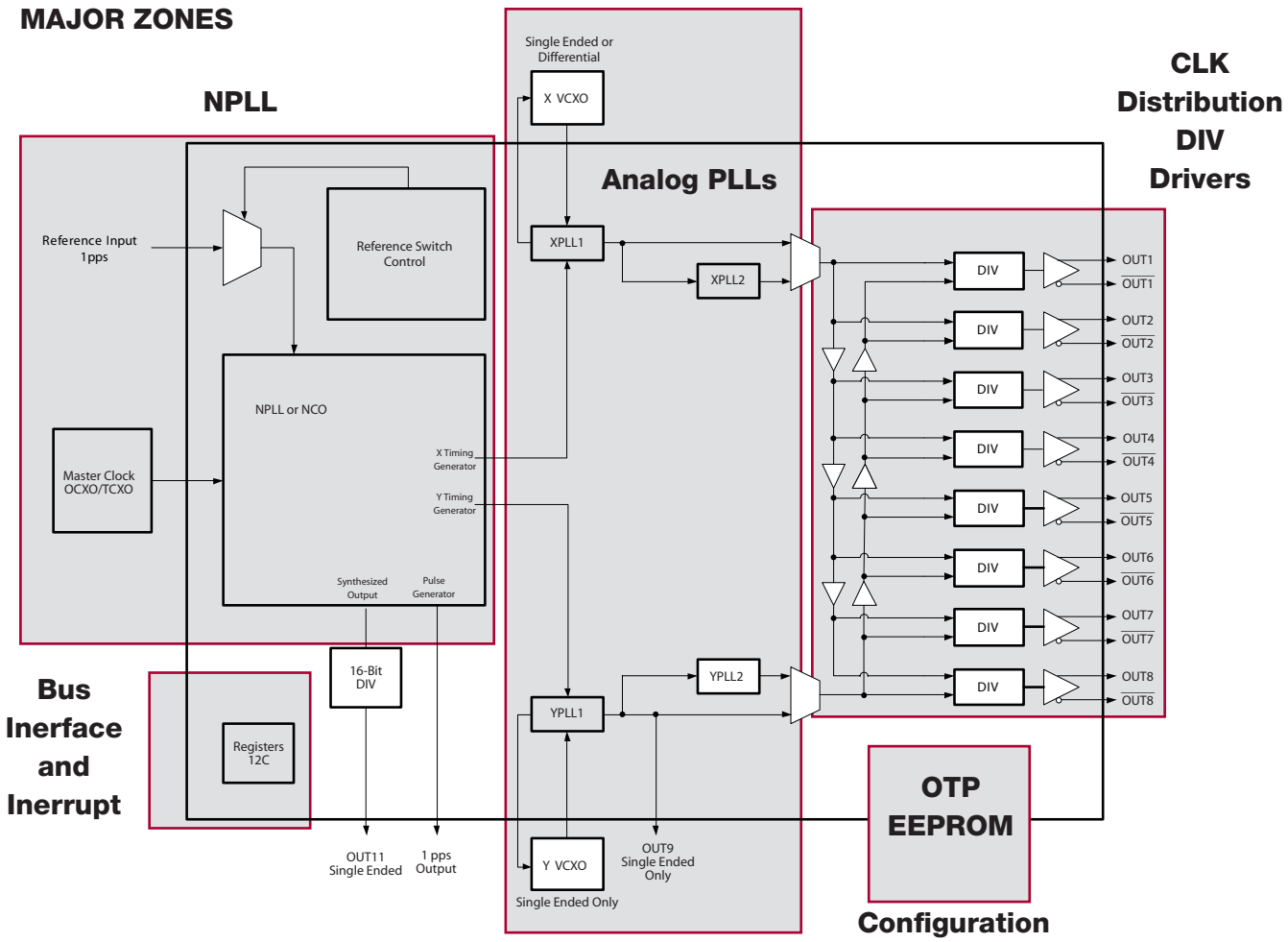
General Description

The NS2D04-1PPS is a highly integrated PLL time and frequency synchronizing integrated circuit that receives a single 1PPS reference input and generates multiple outputs locked to the rising edge of the 1PPS pulse. The 1PPS reference can be generated from a GNSS source. The chip is capable of correcting for the 1PPS signal's quantization error effectively reducing the saw tooth error typically found on GNSS receiver generated 1PPS signals.

The design architecture incorporates a sophisticated digital and analog PLL scheme to provide up to 18 phase/frequency locked clock outputs at frequencies from 1.5 kHz to 800 MHz including a 1PPS pulse generator output. The system is clocked with an external precision OCXO or TCXO providing the basis for various holdover and free run performance options. A variable bandwidth filter (0.35 mHz to .05 Hz) enables supporting phase locking to high jitter 1 PPS input references to less than 1ns resolution. The phase relationship between the 1PPS input reference and output ports can be controlled with programmable settings.

The chip digitally synthesizes three independent frequencies from the timing generator. The 1 PPS pulse is brought out directly from the NPLL synthesizer and another two outputs function as reference inputs to the two analog PLL chains within the chip. These two signals can be attenuated internally to ultra low jitter levels and provide the source for multiple output clocks in the chip's clock distribution section.

The analog portion of the chip consists of two independent PLL chains (X side and Y side) that attenuate jitter through a variety of optional configurations to achieve the user's desired performance level. The chip can operate with either X side or Y side analog PLLs or outputs can be generated from a combination of both X and Y side. One or two disciplined VCXO(s) provides the output characteristics for phase noise and jitter performance for up to 17 clock outputs (8 differential or 17 single ended) with optional configurations that can provide output jitter performance of less than 100fs RMS over the integration range of 12 kHz to 20MHz. The 1 PPS pulse generator is independently controlled and a 1PPS pulse can be generated in holdover mode.



Internal NPLL and Numeric Timing Generator

The kernel of the NS2D04-1PPS is a digital-based numerical PLL. In its core, all internal modules are either digital or numerical, including the phase detectors, filters, timing generator and clock synthesizers. The pure digital design timing generator allows the NS2D04-1PPS to become an accurate and reliable deterministic system.

The NS2D04-1PPS includes a single timing generator. This timing generator can individually operate in free run, synchronized, and holdover mode. The timing generator must be placed in either external-timing mode or self-timing mode via register settings. External timing mode supports “synchronized” mode. In external timing mode, the systems NPLL phase locks to the 1 PPS external reference input. In “synchronized” mode, the NS2D04-1PPS’s PLL loop bandwidth may be programmed from <1mHz to .05 Hz to vary the timing generator’s filtering function.

Self-timing mode supports “free run” and “holdover” modes. In self-timing mode, the PLL simply tunes the clock synthesizers to a given fractional frequency offset. When the 1PPS reference input and previous holdover history are unavailable, such as in system’s initialization stage, free-run mode will be entered and used. When the selected reference input is unavailable but a long-term holdover history accumulated in previous synchronized mode is available, holdover mode may be entered or used. In NS2D04-1PPS, the free-run clock is derived from the MCLK (external oscillator) and digitally calibrated to compensate the external oscillator’s accuracy offset.

Three internal clock synthesizers generate output signals at any frequency (divisible by 8 kHz) from the systems timing generator. Two of these outputs are used internally as reference inputs to the X and Y side analog PLL chain. The output frequency of the synthesizers which support the X and Y side analog PLL chains are register programmable to any frequency divisible by 8 kHz.(8 kHz * M where 1 < M <=5000). The third generates a 1PPS pulse. These synthesized clocks are phase and frequency locked to the internal NPLL.

The system timing generator is supported by an internal numerically controlled oscillator (NCO) that is timed by the systems master clock. The NS2D04-1PPS reports to the user the frequency offset between that of the system master clock and that of the incoming reference in “Locked” mode. When in “holdover” mode, the NCO’s frequency offset can be externally controlled via registers in the chip to calibrate the master clock. This functionality allows the user to externally compensate the NCO output to address drift from temperature fluctuations and/or long term drift characteristics of the external OCXO or TCXO. The NCO offset control has a resolution of less than 1 part per trillion.

Master Clock (MCLK) and Programmable Bandwidth Settings

The system’s master clock (MCLK) requires a “fixed” frequency clock input and is used to clock the NS2D04-1PPS NPLL. The NS2D04-1PPS can be configured to accommodate one of two master clock frequencies – 10MHz or 20 MHz via state settings on pins 36 and 49.

The master clock’s performance characteristics should be consistent with chosen bandwidth settings and desired holdover and free run performance requirements. Bandwidth setting options are programmable in the NS2D04-1PPS from .35 mHz to approximately .05 Hz. When locking to a high jitter 1PPS input signal, a low bandwidth filtering algorithm should be employed using a bandwidth setting in the NS2D04-1PPS below 1mHz. For optimal performance when using low bandwidth settings, the short term stability level of the master clock should be consistent with the Stratum 3E performance requirement. Using a bandwidth setting of .35 mHz and an appropriate master clock, the 20ns jitter from a typical 1PPS GNSS source can be reduced into the range of <1ns. Higher bandwidth settings like .05Hz, can be supported by a TCXO with the appropriate short term stability specification. A variety of master clock options are available from Connor-Winfield to support the NS2D04-1PPS .

The desired frequency input choice is hardware controlled and can be configured by setting the appropriate pins (Pin 36 and Pin 49) to the specific logic level as shown in the table below.

MCLK Frequency Desired	Pin 49 MCLK_Rate 1	Pin 36 MCLK_Rate 0
10.0 MHz	0	0
20.0 MHz	0	1

Table 1 Master Clock Frequency Selection list

Inputs IN1, IN2, IN3

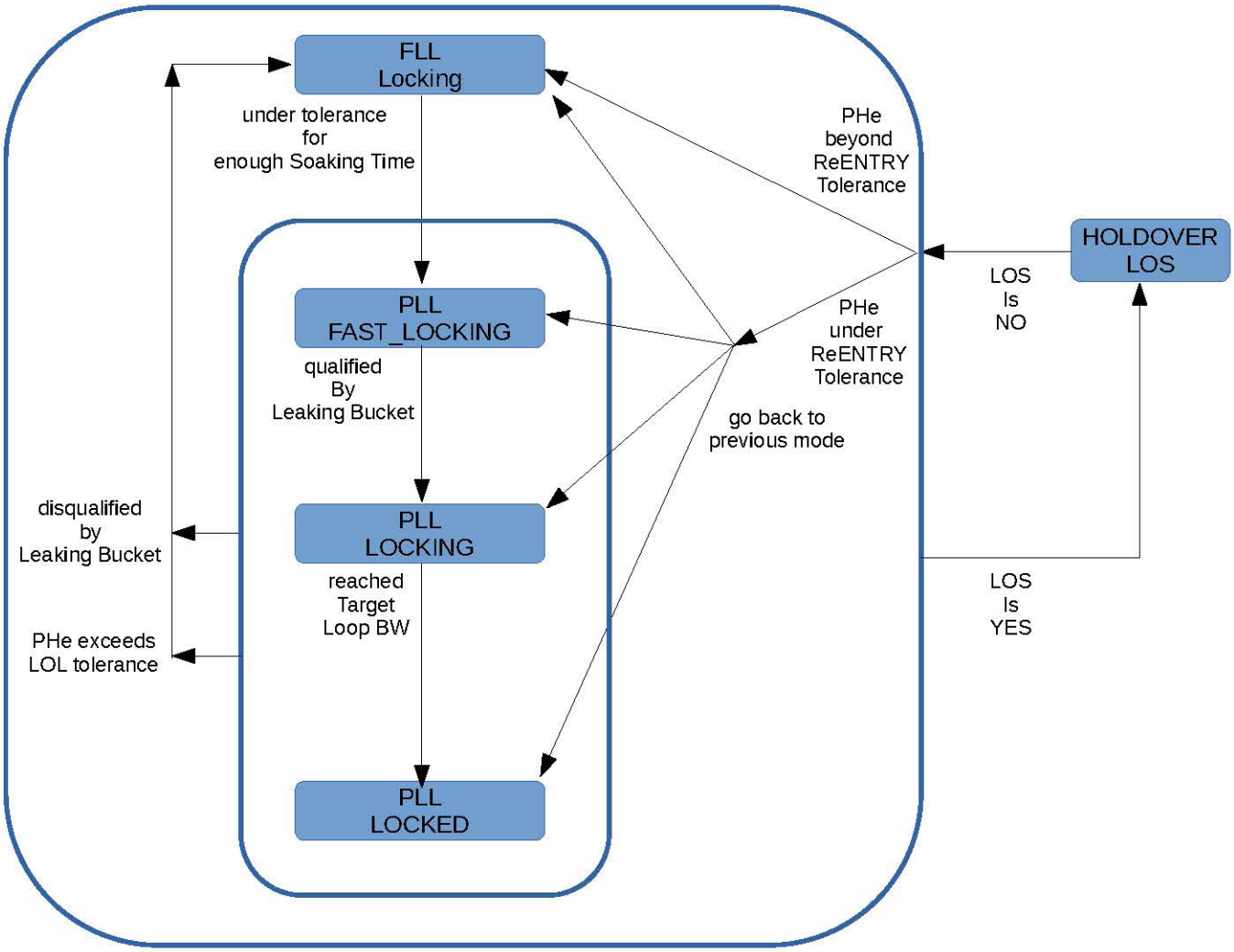
The NS2D04-1PPS has three input ports IN1, IN2 and IN3. However only one port can be chosen at a time to be used as the input to the DPLL. In the 0x35 NPLL_START register, a value is required to start the NPLL. The value chosen determines which input port the 1PPS incoming signal will be arriving on.

Phase Synchronization General

The NS2D04-1PPS digital core generates a synchronized clock, used as the frequency input source for an internal analog, clean up PLL.The synthesized clock output can be programmed to any frequency divisible by 8 kHz to support phase / frequency matching in the downstream analog clean up APLL portion of the IC. In synchronized mode, the phase relationship between the selected reference input and the clock output may be phase arbitrary or frame phase aligned. A zero frame phase relationship is produced by programming in frame phase align mode. An additional synthesized and phase aligned output is the 1 PPS pulse generator.

1PPS Locking and Phase Synchronization Solution

The NS2D04-1PPS phase locking design implementation employs a low bandwidth filtering scheme with multiple locking stages during the complete phase locking process.



Register NPLL_MODE 0x20 provides status of the various locking stages. In addition, this register reports when the fast locking phase is complete and the NPLL is locked to the incoming 1PPS signal and when the phase bias has been eliminated between the phase alignment frequency chosen and the incoming 1PPS signal.

General Theory of Operation: 1PPS Locking and Phase Synchronization Solution

When the NPLL is “kicked up”, the IC starts to operate in IDLE_LOS mode. All the clock/pulse outputs are disciplined by or generated from the external MCLK source, at its initial frequency accuracy, or in conjunction with any user specified frequency offset calibration instructions set in register 0x4F. When the IC detects a valid 1PPS input, it first calculates the real phase position of those input pulses, adjusting for any user specified phase detector calibration setting in register Ox4D, and then measured every period of this 1PPS input.

The NPLL then moves to operate in FLL_LOCKING mode. In this operation mode, the IC adjusts its clock/pulse output frequency attempting to “frequency lock” to the 1PPS input. The user can specify a “soak” time to allow the system to settle. During this soak time, the phase error between the incoming 1PPS and the output 1PPS is measured internally. Cycles where the phase error between the two 1PPS pulses increases, adds to a leaking bucket value. Cycles where the phase error between the two 1PPS pulses decreases, subtracts from the value of a leaking bucket. If the leaking bucket incrementally fills to the threshold level, the soak time counter will reset and begin the FLL process again. If the value of the leaking bucket incrementally reduces to zero level, this indicates that the system has settled down to become frequency locked. At this point, the operation then moves from the frequency locking (FLL) stage to phase locking stage (PLL), starting with a fast locking (PLL_FAST_LOCKING) phase.

The PLL first operates in the PLL_FAST_LOCKING mode, where typically a higher bandwidth value is chosen relative to a “target” or final bandwidth setting at which the NPLL is set to permanently operate at. In the beginning of this stage, a large phase offset can exist between the 1PPS input and IC’s 1PPS output even after the frequency lock loop settles down. In the next 1PPS output, it will jump from its original projected phase position to whatever nearest phase position is estimated to be on the next 1PPS input. The 1PPS output can be controlled through registers so as not to immediately jump to the exact estimated phase position automatically in case the user requests, through register settings, to maintain its phase alignment with some other clock output. The phase difference can be built out over a period of time to avoid introducing an immediate phase hit to the PLL. This PBO (phase build-out) will then be compensated back to the clock/pulse outputs slowly and smoothly out of band without impacting the PLL.

When operating in the FLL and PLL locking modes, the IC employs a “leaking bucket” mechanism which is used to evaluate the phase synchronization condition of the PLL. This condition can be monitored through the registers. The leaking bucket starts at one half of its set value. Based on internal measurements of phase error, the bucket either adds or subtracts a numerical count when each pulse is measured. If the phase error between the incoming 1PPS signal and the 1PPS output increases, it adds one 1 each corresponding second. If the phase error decreases between the input and output 1PPS signal, the bucket value is reduced by one for that pulse. When the bucket is filled beyond the level of its assigned capacity, the system will revert back to the previous locking mode and begin the process again. The leaking bucket threshold level is identified in nS and size of the leaking bucket is an integer number associated with length of time (accumulated 1PPS pulse periods) the user desires to observe prior to allowing the system to the next locking stage.

These design factors are important to consider, based on the bandwidth level chosen and the master clock source. If using an OCXO as the master clock source, an OCXO may take a long time to warm up and settle. When the leaking bucket level is reduced to “0”, indicating the evaluation result is good, the operation mode automatically will move from the fast locking stage to PLL locking stage.

In PLL_LOCKING mode, the “target” PLL loop bandwidth is typically set to a lower loop bandwidth than used in the FAST_LOCKING mode. Based on a user register value specified rate, the system smartly adjusts its PLL loop BW to approach user’s end bandwidth target value. Once the target PLL loop BW is reached and the leaking bucket indicates the result is good, the operation will be labeled as being in PLL_LOCKED mode.

For any reason either if PLL’s leaking bucket mechanism claims a bad phase synchronization evaluation result or if the phase error between the calibrated 1PPS input and the 1PPS output exceeds the user specified loss of lock (LOL) tolerance, the operation mode will be pushed back to FLL_LOCKING mode.

In the case where the 1PPS input signal is lost due to cable disconnection, signal glitches, manually forcing into holdover or any other reason, the operation will be pushed back to the IDLE_LOS mode. The NPLL will work as a holdover clock generator internally, derived solely from the master clock (MCLK) in conjunction with the user’s frequency calibration instructions, if any. When a good quality (valid) 1PPS input signal returns and is present, the phase error between the calibrated 1PPS input and the current 1PPS output will be used determine whether the operation mode should resume to its mode prior to this LOS condition or go to FLL_LOCKING mode directly based on the user defined re-entry phaser error tolerance setting (PHe_ReENTRY_TOLERANCE) in the registers.

PBO and its Compensation

As illustrated previous, a phase built-out may be executed when moving operation from FLL_LOCKING mode to PLL_FAST_LOCKING mode. This phase offset will be compensated back to all the clock/pulse outputs smoothly. Users can specify the maximum limit of the additional frequency offset being applied to all the clock/pulse outputs in order to compensate those phase offset back. The frequency offset acceleration rate is decided by the max allowed additional frequency offset.

$$frequency\ offset\ acceleration = \frac{max\ allowed\ frequency\ offset.}{16.384\ sec}\ ,\ no\ less\ than\ 1\ ppb\ /\ sec$$

The phase shifting to compensate back the PBO phase offset will be smooth. The frequency offset will be speed up in the beginning and stay at its maximum offset if the limit was met. When approaching to its phase offset destination, it will slow down to finally stop at the phase position it targeted. Once all the PBO phase offset being compensated has completed, the PBO compensation "done" status will be claimed. This whole phase shirting process is out-of-band to the PLL, regarding to whatever the PLL's loop bandwidth is.

RUN TIME REGISTERS

The NS2D04-1PPS requires most all NPLL parameters to be set in the registers prior to starting the NPLL using register 0x35 NPLL_KICKUP. Once the NPLL is started, no changes to the register settings will be recognized. However, certain registers are identified in the register description as _RT_ or "run time" registers. Once the NPLL is "kicked up", only NPLL registers identified as _RT_ can be adjusted and recognized by the IC during operation. All non _RT_ registers must be set prior to the kick up of the NPLL. Run time registers were designed and intended to allow the user to monitor the performance of the system and dynamically make adjustments within the system to compensate for those conditions. Examples of the run time registers are: NPLL_RT_PD_CALI (phase adjustement for quantization error correction, NPLL_RT_MCLK_CALI (frequency offset correction), NPLL_RT_PLL_LBW_TARGET (target bandwidth adjustment if locking conditions need real time adjustment).

For all registers requiring setting prior to starting the NPLL, a suggested programming sequence is provided in this document after the register table pages.

The PLL Loop Bandwidth of FAST_LOCKING Mode

The PLL loop bandwidth in FAST_LOCKING mode is programmable. However, the bandwidth should be set no higher than 100 mHz. If this register is set higher than 100 mHz, the register value will be ignored and this bandwidth will stay as 100 mHz.

The Target PLL Loop Bandwidth

The target loop bandwidth is programmable in runtime. This target bandwidth must not be set higher than the bandwidth for FAST_LOCKING mode. Otherwise, the register value will be ignored and the internal target bandwidth will be set to be same as the bandwidth for FAST_LOCKING mode.

Between LOCKING mode and LOCKED mode

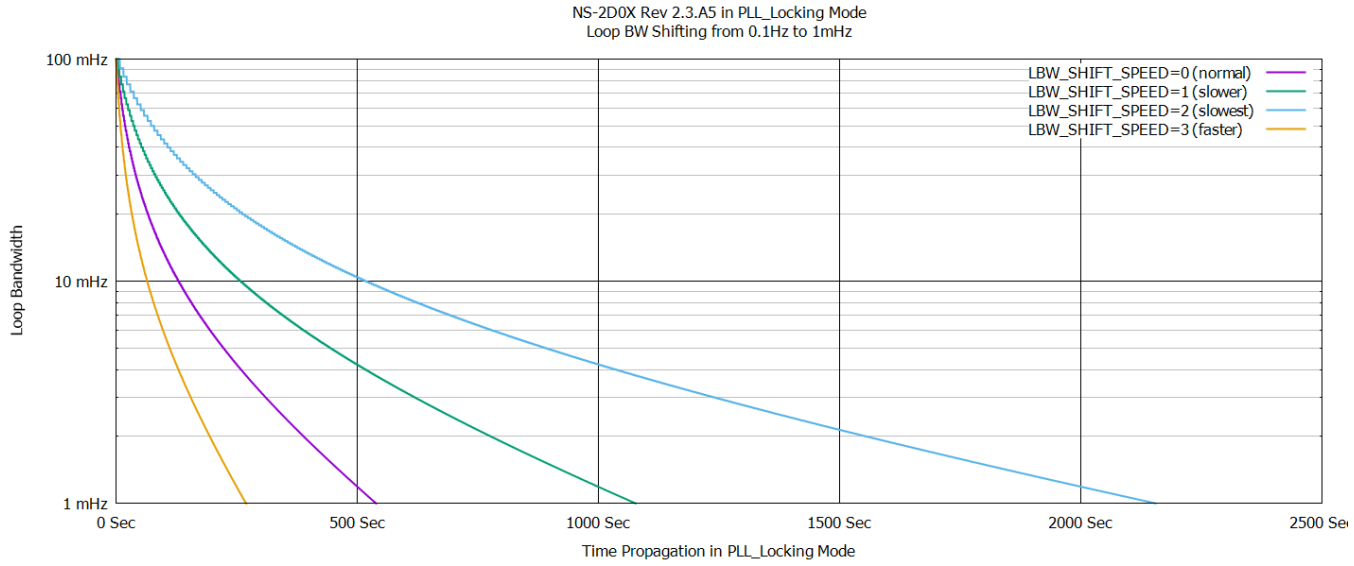
In run time, if the current working PLL bandwidth is no higher than the target bandwidth, the NPLL mode will be promoted from LOCKING to LOCKED. The NPLL mode will be demoted from LOCKED to LOCKING once the target bandwidth is reprogrammed to be lower than the current running bandwidth.

General Theory of Operation: 1PPS Locking and Phase Synchronization Solution continued

LBW Shifting Speed in PLL_Locking Mode

The loop bandwidth shifting speed can be configured in register NPLL_CONFIG. While the NPLL is in PLL_Locking mode, its loop bandwidth will slowly shift into the target normal loop bandwidth at one of four shifting speeds as chosen in register NPLL_RT_PLL_LBW_TARGET. The bandwidth shifting speed is not linear.

LBW Shifting from 100mHz down to 1mHz



PHe Tolerances

The system monitors the difference between the phase eror of the incoming 1PPS signal the the 1 PPS Output signal. The user determines the phase error tolerance level to initiate a loss of lock (LOL) condition using register NPLL_RT_Phe_LOL_TOLERANCE. The user also determines the re-entry phase erorr threshold level for avoiding re-starting in FLL_Locking Mode if the phase error stays within a given range during holdover periods. Register NPLL_RT_PHe_ReENTRY_TOLERANCE ais used to set this level. Please note that both registers are run-time registers for dynamic runtime control.

PLL modes and Leaking Bucket operation

While promoting the operation mode, the loop bandwidth will be switched to the relative loop bandwidth preassigned to that mode. The system uses one leaking bucket to promote from PLL_ FAST_LOCKING to PLL_LOCKING and to claim the LOL events. While promoted from PLL_FAST_LOCKING to PLL_LOCKING, the loop bandwidth will migrate from PLL_FAST_LOCKING's loop bandwidth to the target loop bandwidth slowly and smoothly following the speed rate user specified. After reaching the "target" normal loop bandwidth, the operation mode moves to PLL_LOCKED. The exact running PLL loop bandwidth at any moment could be read out from register (NPLL_PLL_LBW_IDX_NOW).

ReENTRY from Holdover/LOS mode

The phase error between the 1PPS_IN and 1PPS_OUT, will dictate how the system recovers from an LOS or Holdover mode condition. If the measured phase error is beyond the ReENTRY threshold, level set in the registrers, the system will revert to FLL locking mode. Otherwise, the system will go back to the mode prior to entering HOLDOVER mode due to LOS events.

From FLL Locking to PLL Locking

The criteria to promote the NPLL mode from FLL locking to PLL locking is to continually have a given quality condition to be satisfied for a certain soaking time. Any condition violation resets the soaking time counter. The mechanism measures the peak-to-peak frequency offset (versus the calibrated MCLK) on the FLL output and must maintain within the given frequency tolerance.

The PLL Loop Bandwidth of FAST_LOCKING Mode

The PLL loop bandwidth in FAST_LOCKING mode is programmable. However, the bandwidth should be set no higher than 100 mHz. If it was, the register value will be ignored and this bandwidth will stay as 100 mHz.

General Theory of Operation: 1PPS Locking and Phase Synchronization Solution continued

The Target PLL Loop Bandwidth

In run time, if the current working PLL bandwidth is no higher than the target bandwidth, the NPLL mode will be promoted from LOCKING to LOCKED. The NPLL mode will be demoted from LOCKED to LOCKING once the target bandwidth is reprogrammed to be lower than the current running bandwidth.

Between LOCKING mode and LOCKED mode

In run time, if the current working PLL bandwidth is set no higher than the target bandwidth, the NPLL mode will be promoted from Phase LOCKING to Phase LOCKED. The NPLL mode will be demoted from LOCKED to LOCKING once the target bandwidth is reprogrammed to be lower than the current running bandwidth.

Holdover and Loss of Signal (LOS)

Holdover mode is available after the system has successfully locked to a valid 1PPS reference input signal. There are two ways in which the system can move into holdover mode. Register 0x36 [7:0] NPLL_RT_CTRL allows the user to manually force the system into a Loss of Signal (LOS) mode. The other is when the system detects that no signal exists on the incoming reference. This condition will put the system into Holdover mode automatically. Through its internal counter, the NS2D04-1PPS can detect the existence of a 1PPS signal, however, it does not perform any qualification evaluation of the validity of the 1PPS signal.

In return from Holdover mode, the NS2D04-1PPS design allows the user to set phase error tolerance threshold levels to control the sequence when re-entering the locking process.

Phase Detector Calibration/Saw Tooth Error Correction

The NS2D04-1PPS provides access to the chip's internal phase detector to enable dynamic adjustment to address and correct for the saw tooth noise and adjust phase offset due to antennae cable runs. In dynamic use, the register value must be ready when its associated 1PPS input pulse arrives. The readiness of this register's value must be compliant to a minimum set time (10uS) and hold time (125 uS). Generally, calibrating quantization error reported by the GNSS receiver is the primary use for this register's functionality.

Frequency Offset Calibration

The NS2D04-1PPS provides the user an ability to digitally fine tune its internal master clock. The calibration range is ~ ± 114 ppm. The internal master clock is boosted in frequency from the external clock source used. In holdover mode, this feature can be used to accommodate for predictable drift in the external clock to compensate for changes in frequency due to temperature change or long term drift due to aging. Using an OCXO that has been designed for temperature coefficient correction can be used in conjunction with this feature. This feature provides the user a resolution of < 1 ppt per step. Negative values decreases the frequency. Positive values increases the frequency.

EVENT_INTR

The NS2D04-1PPS provides an event interrupt notification function (EVENT_ INTR pin 4). This pin's sole function is to notify the user when the NPLL_MODE status changes.

In this one bit register, the interrupt pin becomes "active" when at least one bit is non-zero. The current interrupt status can be read from this register. Once the interrupt pin is activated, it can only be deactivated when the interrupt status has been erased. The user can write to this register, however, its operation is not “write-the-value- then–replace-the-value”. It is a bit-operation. For each bit, write “1” to erase that bit value. It can be stated as: INTR_STATUS = INTR_STATUS & (~VALUE).

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x07~0x08	[15:0]	INTR_EVENT	RW	0	Interrupt Event bit[0] REG(NPLL_MODE) value changed bit[15~1] ~ RSVD ~

1PPS Output

The 1PPS output’s pulse width can be programmed in the NS2D04-1PPS.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0xA0~0xA1	[11:0]	1PPS_PULSE_WIDTH	RW	10	1PPS output pulse width. Unit in uS.

Synthesized Output 11

The NS2D04-1PPS provides a programmable LVCMOS 3.3V output that can generate clock frequencies from ~152Hz to 80 MHz. An initial stage at register 0xA7~0xA8 allows the user to generate an 8kHz divisible frequency from 10MHz to 80MHz. Through the use of a 16 bit post divider at register 0xA9~0xAA, frequencies generated in the initial stage can then be further integer divided to a lower frequency by setting a value in the post divider register. However, only frequencies divisible by 8kHz can be phase aligned to the rising edge of the incoming 1PPS signal.

Phase Alignment to Clock Outputs

The NS2D04-1PPS can be configured to phase align the rising edge of incoming 1PPS signal with the rising edge of the frequency outputs generated in the two analog PLL chains, OUT_11 driven by the synthesized outputs from the NPLL’s timing generator, and the rising edge of the 1PPS output. For alignment to occur however, frequencies generated must be integer divisible by 8kHz. A valid frequency must be reported in register 0x46~4B and a valid phase build out rate must be entered into register 0x4C in order for the phase alignment function to successfully operate. If generating multiple outputs at different frequencies, the highest common divided integer frequency among the output frequencies generated should be chosen to be input into the NPLL_RT_ALIGNED_OUT_FREQ register. Frequencies identified in the NPLL_RT_ALIGNED_OUT_FREQ register can be chosen as low as 8kHz for purposes of finding a common related frequency. Both or either X and Y side APLL chains can be set to align with the 1PPS signal.

Once the NPLL is started using register NPLL_START, a phase build out process begins to bring the clock output into phase alignment with the rising edge of the incoming 1PPS signal. A default phase error build out rate can be chosen between 10 pS/S and 2.55 nS/S. When very low frequencies are to be generated, a "wide range" mode can be enabled to increase the speed of the phase build out rate. The build out rate is set in the NPLL_PHASE_SHIFT_SPEED register, depending upon using default or Align-in-Wide-Speed mode.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x45	[7:0]	NPLL_CONFIG	R/W	0	NPLL’s phase align configuration bit[0]: Phase aligned to 1PPS on XPLL: 1=YES, 0=NO bit[1]: Phase aligned to 1PPS on YPLL: 1=YES, 0=NO bit[3:2]: PLL_LBW_SHIFT_SPEED To specify the LBW shifting speed in PLL_LOCKING mode from LBW(FAST_LOCKING) to LBW (NORMAL) 0: normal 1: slower 2: slowest 3: faster bit[7:4]: ~RSVD~
0x46~4B	[47:0]	NPLL_RT_ALIGNED_OUT_FREQ	R/W	0	The frequency of output to align to 1PPS output. 17-bit. Unit in 8kHz. bit [16:0] n, freq = 8kHz x n bit [47:17] must be zero

NS2D04-1PPS Analog PLL Chain General Description

The NS2D04-1PPS supports two independent analog PLL chains (X,Y) to support two simultaneous, independent frequency domains that share ten programmable clock output transmitter ports. There is an additional single ended output on the Y-side (Output 10). The NS2D04-1PPS consists of two (2) independent sets of two (2) cascaded PLL stages, referred to as the X and the Y side. In each X and Y side of the chip, the first stage PLL (XPLL1 and YPLL1) attenuates the initial jitter from the reference input/NPLL with the use of an external VCXO.

When in operation, the locked VCXO signal can be sent directly to the output transmitter ports for a direct pass through of the VCXO frequency or further divided using the independent 20 bit divider circuits at each output transmitter port.

Alternatively, the VCXO frequency/signal can be sent to a second stage PLL. A second stage PLL for each X and Y side (XPLL2 and YPLL2) with an integrated high frequency VCO is available to accept the output of the first stage PLL1. Each PLL2 has an integrated phase frequency detector, charge pump and VCO in the usable range of 1.2GHz to 1.475 GHz that can be employed to generate locked output clocks at the eight output transmitter ports using the eight independent 20 bit divider circuits found at each transmitter ports.

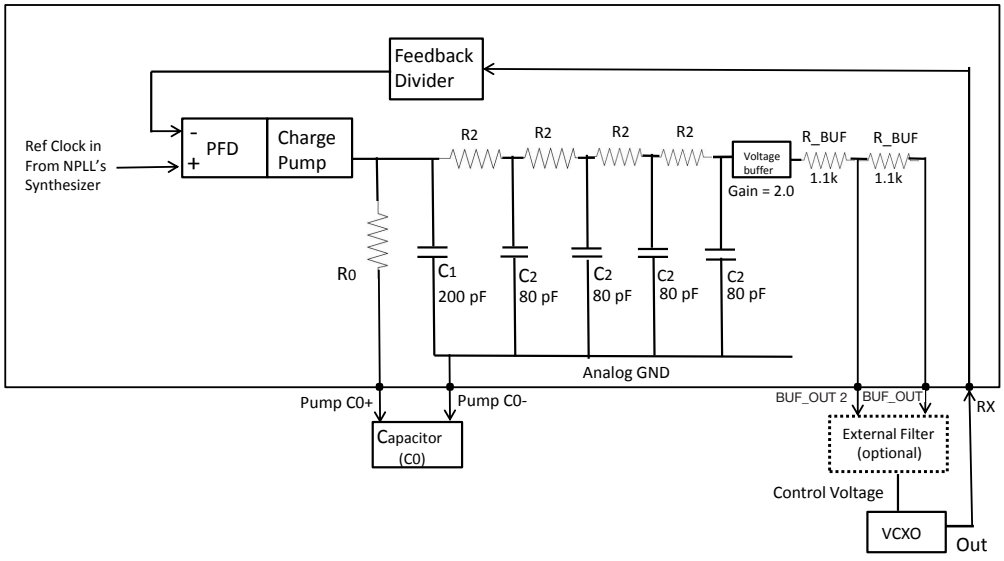
This design architecture gives the user a great deal of control over the output phase noise and jitter level generated by the NS2D04-1PPS . An external VCXO with exceptional phase noise and jitter performance can be used in bypass mode of the NS2D04-1PPS to retain the ultra-low jitter performance characteristics with very little additive jitter contributed by the NS2D04-1PPS . Low frequency VCXO sources (as low as 1 MHz) as well as differential clock sources (up to 800 MHz) can be used in bypass mode to achieve maximum jitter attenuation. If outputs are generated using PLL2, single ended VCXOs at frequencies between 40 MHz and 100 MHz should be used for best performance. Depending upon the external VCXO configuration used, clock outputs can be generated in the frequency range from 1Hz to 800MHz, limited to 180MHz for LVCMOS outputs.

PLL1 (X,Y) General Description

PLL1's (X,Y) function in the NS2D04-1PPS it to act as a frequency translator and jitter attenuator. PLL1(X,Y) effectively attenuates the jitter from the incoming reference clock and translates the frequency to that of the chosen external VCXO which supports it. PLL1(X,Y) can pass through the external VCXO frequency directly to the output dividers and transmitters or be used as the input frequency to the second stage PLL, PLL2 (X,Y). When the VCXO clock output is passed directly through to the output dividers and transmitters, the NS2D04-1PPS is capable of attenuating the jitter with approximately 10fs additive jitter to that of the external 3.3V VCXO.

PLL1(X,Y) consists of a phase-frequency detector (PFD), charge pump, passive loop filter, and an external VCXO operating in a closed loop. PLL1(X,Y) has the flexibility to operate with a loop bandwidth of approximately 10Hz to 200 Hz. This relatively narrow loop bandwidth gives it the ability to suppress jitter that appears on the synthesized clock signal feeding PLL1 from the NS2D04-1PPS 's NPLL. This synthesized clock eliminates the requirement for a phase detector frequency relationship between the frequency of the reference inputs into the NS2D04-1PPS and the output VCXO frequency desired. The NPLL's synthesizer frequencies are programmable allowing for a flexible phase detector rate however the PFD rate must be divisible by 8kHz (8 kHz * M where <1 M <=5000). The charge pump current ,feedback divider, R0,and R2 are register programmable inside the chip. Capacitors C1 and C2 are internal and are fixed values. One external capacitor is required for the NS2D04-1PPS's loop filter, which connects to pins Pump_C0+ and Pump_C0- . An optional external filter on the control voltage pin of the external VCXO is supported through BUF_OUT2 and BUF_OUT pins.

PLL 1 Circuit Diagram (X , Y)

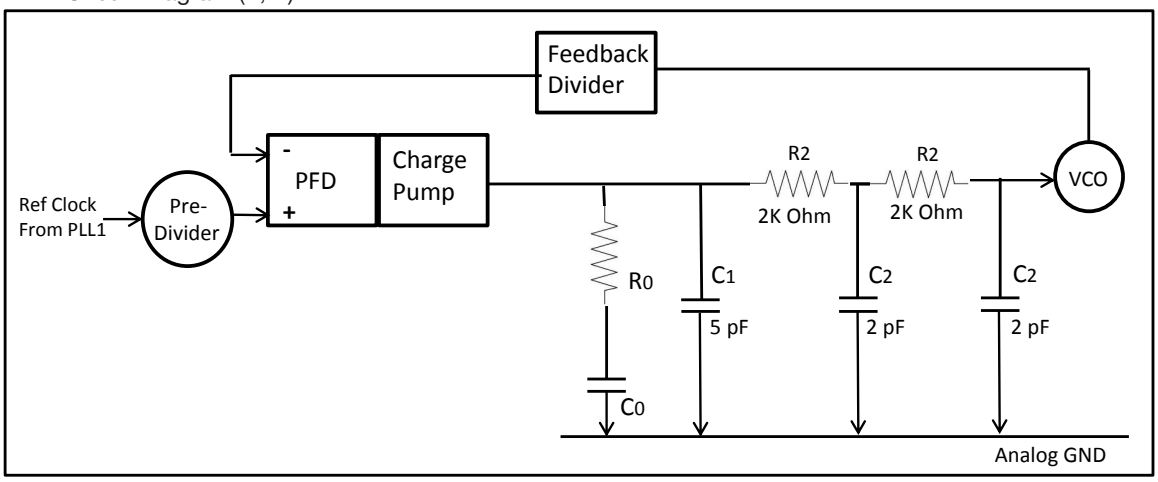


PLL2 (X, Y) General Description

PLL2 (X,Y) operates as a second stage analog PLL block, taking its reference input directly from PLL1 (X,Y). PLL2 (X,Y) consists of a fully integrated phase-frequency detector (PFD), charge pump, integrated loop filter, and integrated internal VCO operating in a closed loop. The NS2D04-1PPS 's internal VCO operates in the effective frequency range from 1.2GHz to 1.495GHz. Due to the wide range of frequency options of the VCXO input into PLL1 (X,Y), a pre-divider is made available for PLL2. The VCXO frequency used in PLL1 (X,Y) is usually used as the reference frequency into PLL2 (X,Y), however if the VCXO frequency used in PLL1 (X/Y) is greater than 180MHz, the PLL2 (X,Y) pre-divider should be used to keep the input frequency to PLL2 (X,Y) to less than 180 MHz. Once the input frequency into PLL2 (X,Y) has been determined, the appropriate feedback divider value should be chosen match the input frequency to the VCO frequency in the NS2D04-1PPS's usable range. When setting up the registers for PLL2 (X,Y), it is important to note that the values of the registers for setting up PLL1 (X,Y) and PLL2 (X,Y) should be completed and set, including pre-divider and feedback divider for PLL2 (X,Y) prior to initiating the X and Y PLL MODE register setting (0x05 and 0x06). This sequence of operation is required for an automatic self calibration necessary to ensure proper locking of PLL2 (X,Y) to the incoming reference signal from PLL1 (X,Y).

Once PLL2(X,Y) is properly locked, the chosen VCO frequency can be integer divided using the 20 bit programmable post-divider circuits preceding the programmable output transmitter ports. The charge pump current, feedback divider, R0, C0 and the Kvco of the internal VCO are register programmable inside the chip and can be updated/changed during operation after the PLL is locked successfully. Capacitors C1 and C2 and R1 are predefined fixed values.

PLL2 Circuit Diagram (X, Y)

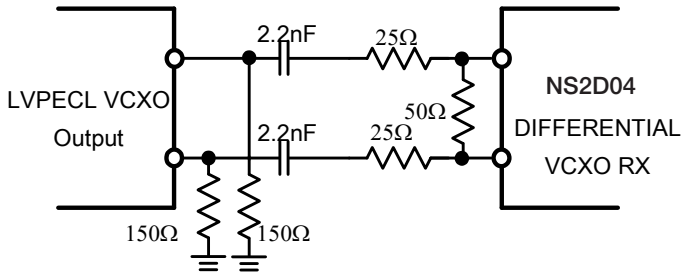


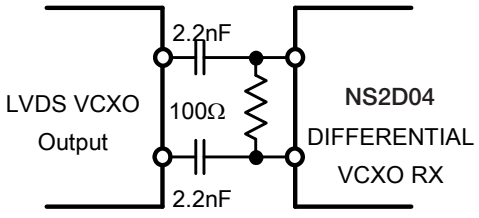
X-Side PLL Chain

On the X side of the chip, XPLL1 can be supported by a single ended or differential VCXO at frequencies from 10MHz to 800MHz.. Well-chosen high frequency VCXOs can provide jitter performance levels in the 50 to 60fs range and thus locked outputs from XPLL1 can provide well under 100fs jitter performance levels in the integration band of 12 kHz to 20MHz. This frequency can then be passed through to additional output transmitters/dividers and/or be used as an input to the second stage PLL (XPLL2) to synthesize additional output frequencies at the output transmitter ports. Outputs derived from XPLL2, depending upon frequency, will generally provide jitter performance levels of < 300fs over the integrated band of 12kHz to 20 MHz.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION	
0x05	[2:0]	XPLL_Mode	RW	0	XPLL Mode	
					0,5,6,7:	Both XPLL1 and XPLL2 are power down
					1:	XPLL1 with sgl VCXO -> XPLL2
					2:	XPLL1 with diff VCXO -> XPLL2
					3:	XPLL1 with sgl VCXO; XPLL2 is power down
					4:	XPLL1 with diff VCXO; XPLL2 is power down

Differential VCXO termination recommendation in to pins XRX_P and XRX_N





Y-Side PLL Chain

On the Y side of the chip, YPLL1 can be supported only by a single ended VCXO at frequencies from 10MHz to 160MHz. At Output 10, the VCXO nominal frequency will bypass directly to Output 10 in order to optimize clock jitter performance with a minimal additive jitter from the chip. Output 9 is LVCMOS only which effectively acts as a buffer from the VCXO in and directly out of the chip to achieve optimal jitter (usually less than 10fs additive jitter) for ultra-low jitter applications. A well-chosen high frequency LVCMOS VCXO can provide jitter performance levels in the 60 fs range and thus locked outputs from YPLL1 can provide well under 80fs jitter performance levels in the integration band of 12kHz to 20MHz This VCXO frequency can then be passed through to additional output transmitters/dividers and/or be used as an input to the second stage PLL (YPLL2) to synthesize additional output frequencies at the output transmitter ports. Outputs derived from YPLL2, depending upon frequency, will generally provide jitter performance levels of < 300fs over the integration band of 12kHz to 20 MHz.

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
0x06	[2:0]	YPLL_Mode	RW	0	YPLL Mode 0,5,6,7: Both YPLL1 and YPLL2 are power down 1,2: YPLL1 with sgl VCXO -> PLL2 3,4: YPLL1 with sgl VCXO; YPLL2 is power down

Clock Distribution, Dividers and Drivers

The NS2D04-1PPS generates up to 23 clock outputs on ten output transmitter ports and three single ended 3.3V clock output pins driven from various sections of the chip. Output transmitter ports 1-8 are preceded by a 20 bit divider circuits (any integer value from 1-1,048,576). The divider circuits can be used regardless whether the output were generated from PLL1 or PLL2.

Output transmitter ports 1 through 8 are driven by clocks generated from PLLs 1 or 2 on either the X or Y side of the chip. Output transmitter ports 0 and 10 serve only their respective X and Y side of the chip. The output transmitter ports consist of programmable 3-in-1 transmitters that can be configured to output either (2) LVCMOS or 1 LVDS or 1 LVPECL logic signal. Output transmitters can be powered down if not in use. When using LVCMOS mode, outputs can be generated on both output pins (P and N) of the output transmitter, or, one or the other. Polarity of the LVCMOS output at each pin is controllable.

Output 9, on the Y side of the chip, has been provided for use as a low jitter buffer that directly bypasses the Y side VCXO signal in and out of the chip resulting in the least amount of additive jitter (about 10fs). This output is intended to be used for ultra-low jitter performance requirements but will have inverted phase from the outputs that are generated through the transmitter output ports.

The NS2D04-1PPS also has a 1PPS pulse generator which outputs a programmable pulse width 3.3V CMOS 1PPS signal which is also derived directly from the system's timing generator.

Output 11 is a 3.3V single ended CMOS output clock that has been provided to allow for an "any frequency" output that is synthesized directly from the NS2000-1PPS NPLL's timing generator. This output, because it is digitally synthesized, will have higher jitter than Outputs 0-10. Output 11 has a frequency range of 10MHz to 80MHz and is programmed as 8kHz * M where 1250 <= M <= 10000.

Output Bank Details and Constant Skew Delay Description

Output transmitter ports 1 through 8 are divided into four output “banks”. Each of the four output banks must be controlled as a unit. Bank0 (Output transmitters 1 and 2), Bank1 (Output transmitters 3 and 4), Bank2 (Output transmitters 5 and 6), and Bank3 (Output transmitters 7 and 8) represent four “banks” of outputs that can be controlled independently from each X and Y side of the chip. Either the X side or the Y side of the chip can access all four output banks, thus eliminating the requirement to use both sides X and Y in all applications. However, X and Y side clock signals must access output banks in order and must stop at the first output bank placed in use by the alternate side. For example, if X side uses banks 0, 1 and 2, Y side can only access bank 3 (outputs transmitters 7 and 8) or if Y side uses banks 3 and 2 (output transmitters 8,7 and 6,5), X side can only access bank 1 and 0 (outputs transmitters 1,2 and 3,4).

Registers 0xA4,0xA5 and 0xA6 support this function.

The skew between clock outputs is constant but will exhibit a cumulative delay relative to each other based on the clock signal traveling through MUXs and Buffers. This will be dependent upon how the output banks are configured from each X and Y side. Delay times are identified in Diagram 1. The phase skew alignment of the reference inputs to the X and Y side VCXO can be programmed to a zero level using register settings.

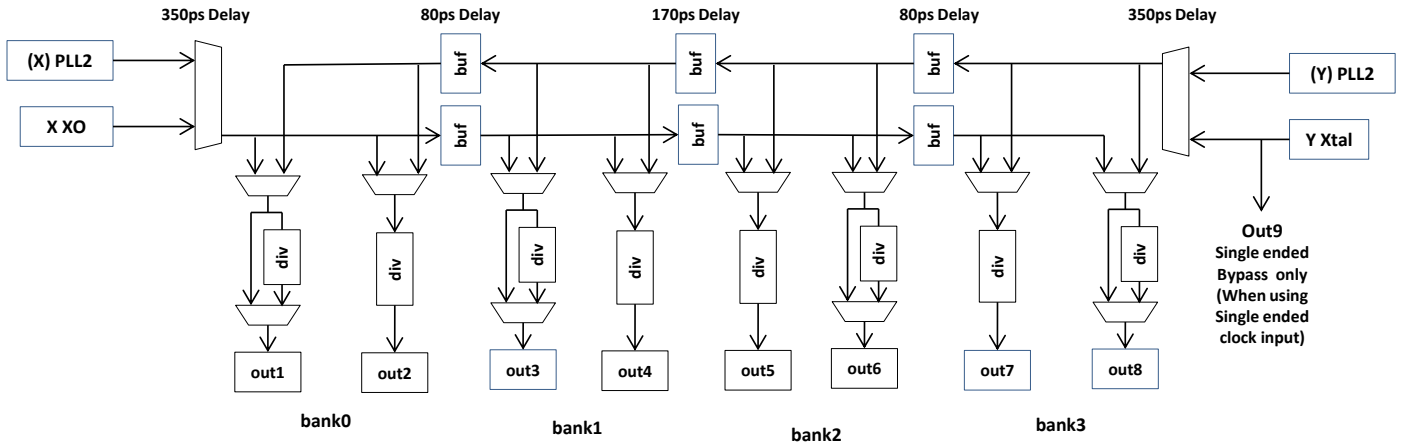


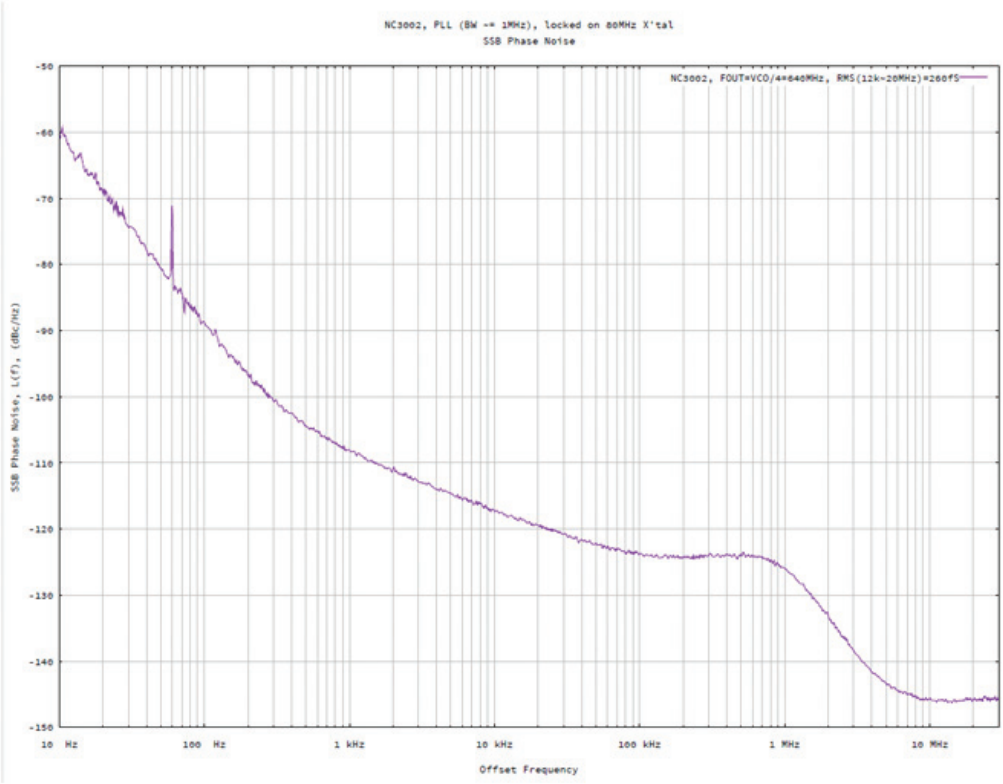
Diagram 1 Detailed Output Banks and Ports Diagram

Symmetry Control for low value odd dividers

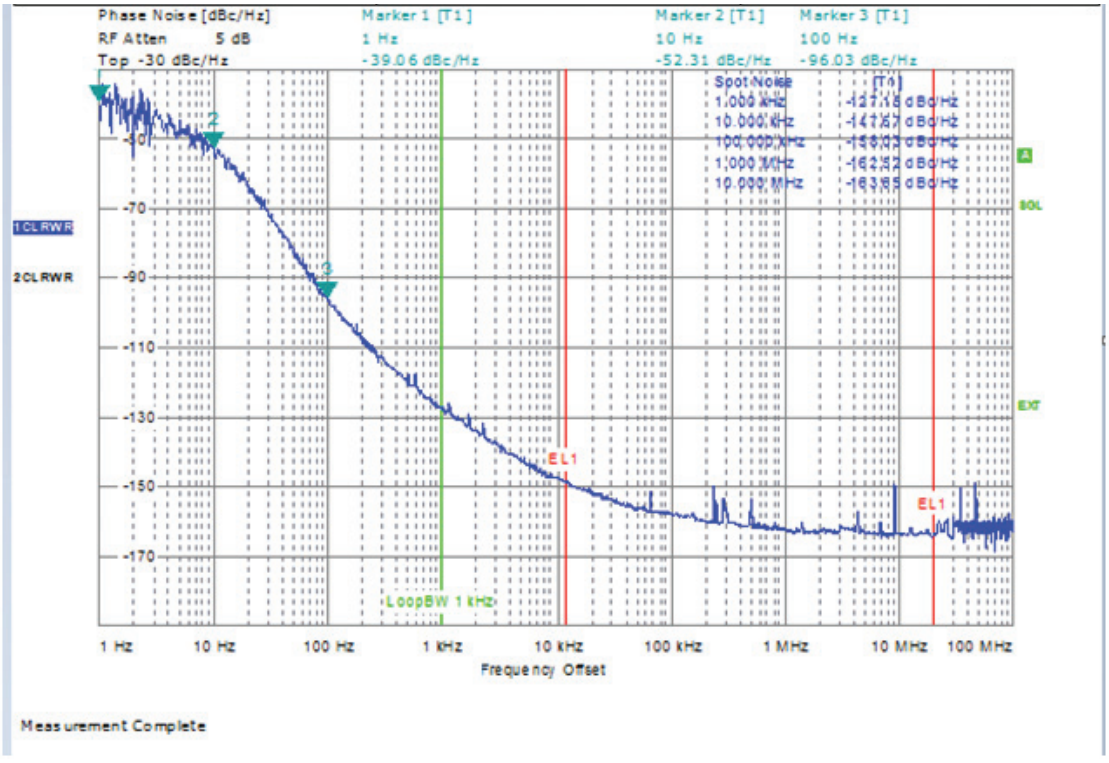
Due to overall power limitations in the chip, only output transmitter circuits 2, 4, 5 and 7 have, by default, output symmetry control when dividing by a low, odd integer value. In circumstances which require dividing the VCO output frequency by values of 3, 5, 7 or 9, one of these output transmitter circuits should be used to achieve 50/50 duty cycle. When using an odd divider value of greater than nine (9), symmetry control is generally not required to maintain reasonable symmetry in the output. The output ports offering symmetry control do not allow for a direct by-pass through of the reference input frequency and require dividing at the output transmitter circuit by a minimum by 2. Output ports 1, 3, 6 and 8 can by-pass the divider circuit entirely or can divide by any integer number up to the 20bit value.

Output Phase Noise Characteristic Examples:

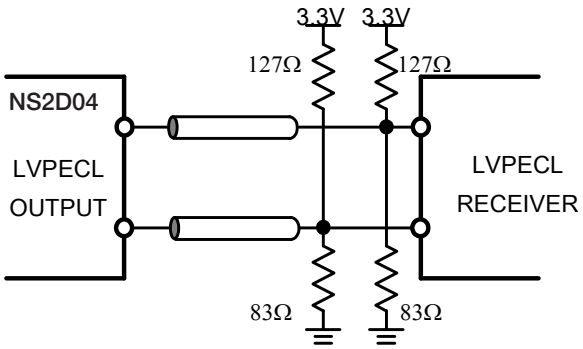
Phase noise generated from PLL2: 640MHz using 80MHz VCXO 260fs (12kHz-20MHz)



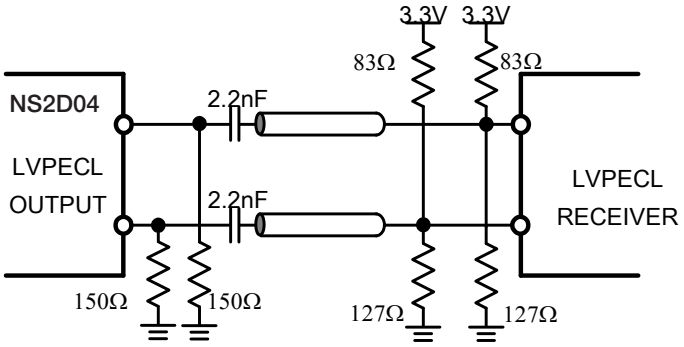
Phase noise generated from PLL1(y): 122.88MHz 63fs (12kHz-20MHz) (using Connor Winfield model V7223T-122.88MHz LVCMOS 5x3.2mm VCXO)



NS2D04-1PPS LVPECL Suggested Termination



DC-Coupled LVPECL Termination

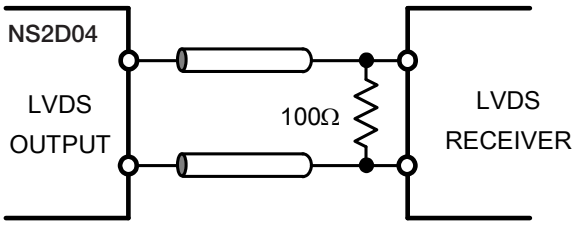


AC-Coupled LVPECL Termination

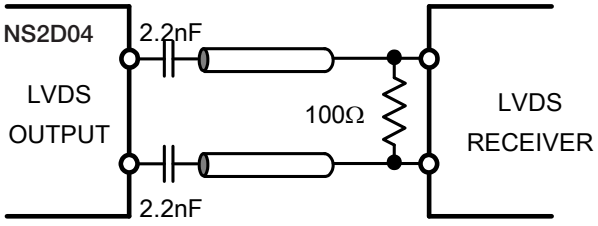
LVPECL Current Consumption
fvco=1.244GHz, fvcxo=38.88MHz,ftcxo=20MHz

OUTPUT FREQUENCY (MHz)	DUTY CYCLE (%)	RISE TIME (20%~80%)(ps)	CURRENT CONSUMPTION (mA)	DIFFERENTIAL SWING (Vp-p)
38.88	50.09	590	41.69	1.183
103.681	49.97	570	41.59	1.139
113.108	45.44	560	41.59	1.148
124.417	49.98	570	41.57	1.161
138.239	44.49	520	41.53	1.171
155.519	49.98	530	41.56	1.152
177.74	43.06	570	41.56	1.163
207.362	50.1	510	41.41	1.182
248.836	42	430	41.34	1.095
311.054	50.14	500	41.32	1.049
414.736	35.64	370	41.53	0.86
622.115	51.05	270	41.56	0.778

NS2D04-1PPS LVDS Suggested Termination



DC-Coupled LVDS Termination



AC-Coupled LVDS Termination

LVDS Current Consumption
fvco=1.244GHz, fvcxo=38.88MHz,ftcxo=20MHz

OUTPUT FREQUENCY (MHz)	DUTY CYCLE (%)	RISE TIME (20%~80%)(ps)	CURRENT CONSUMPTION (mA)	DIFFERENTIAL SWING (Vp-p)
38.8815	49.97	700	18.18	0.593
103.68	50.18	620	18.26	0.586
113.107	50.46	600	18.26	0.593
124.414	50.21	610	18.26	0.606
138.241	50.52	580	18.26	0.61
155.52	50.26	600	18.26	0.6
177.737	50.81	610	18.26	0.598
207.363	50.52	600	18.25	0.623
248.832	50.8	450	18.25	0.575
311.05	50.62	580	18.26	0.547
414.733	49.57	250	18.27	0.431
622.108	50.9	220	18.24	0.378

NS2D04-1PPS Register Table

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
Revision					Chip ID, it reflects the current product ID
0x00~0x01	[15:0]	Chip_ID	R	0x2D00 0x2D04	0x2D00: 88-pin NS2D00r2 0x2D04: 68-pin NS2D04r2
0x02	[7:0]	Chip_REV	R	0x02	Chip Revision
0x03	[7:0]	Chip_Sub_REV	R	0x03	Chip Sub Revision
0x04	[7:0]	NPLL_FW_REV	R	10	NPLL's Firmware Revision
0x10~0x11	[15:0]	1PPS_IN_COUNT	R	0	The 1PPS_IN receive count. Overflown will truncate back to zero.
0x12~0x13	[15:0]	1PPS_OUT_COUNT	R	0	The 1PPS_OUT transmitted count. Overflown will truncate back to zero.
0x14~0x15	[15:0]	NPLL_PLL_LBW_IDX_NOW	R		To indicate NPLL's current PLL_LBW_IDX for operating in PLL_FAST_LOCKING, PLL_LOCKING, and PLL_LOCKED modes.
0x16~0x1F	RSVD ~				
System					XPLL Mode 0,5,6,7: Both XPLL1 and XPLL2 are power down 1: XPLL1 with sgl VCXO -> XPLL2 2: XPLL1 with diff VCXO -> XPLL2 3: XPLL1 with sgl VCXO; XPLL2 is power down 4: XPLL1 with diff VCXO; XPLL2 is power down
0x05	[2:0]	XPLL_Mode	RW	0	
0x06	[2:0]	YPLL_Mode	RW	0	YPLL Mode 0,5,6,7: Both YPLL1 and YPLL2 are power down 1,2: YPLL1 with sgl VCXO -> PLL2 3,4: YPLL1 with sgl VCXO; YPLL2 is power down
0x07~0x08	[15:0]	INTR_EVENT	RW	0	Interrupt Event bit[0] to indicate REG (NPLL_MODE) value changed bit[14~1] ~ RSVD ~
0x09~0x1F		~ RSVD ~			
NPLL					NPLL_MODE bit {2:0} NPLL's operation mode 0: HOLDOVER_LOS 1: FLL_LOCKING 2: ~ RSVD ~ 3: PLL_FAST_LOCKING 4: PLL_LOCKING 5: PLL_LOCKED 6,7: ~ RSVD ~ bit[6:3]: ~ RSVD ~ bit[7]: NPLL's z[np vp,[rmdsyopm status 0: the compensation is not completed yet 1: the compensation was done
0x20	[7:0]	NPLL_MODE	R		
0x21~0x22	[15:0]	NPLL_INFO_EX	R		16-bit NPLL Extra Information. It could have different meaning in different NPLL_MODE if in FLL_LOCKING mode bit[14:0] countdown of soaking time, unit(S) bit[15] == 0 if in PLL_FAST_LOCKING, PLL_LOCKING, and PLL_LOCKED mode. bit[14:0] leaking bucket's level bit[15] == 1
0x23~0x28	[47:0]	PHe_RAW	R		Raw phase error between 1PPS output and 1PPS input. 48-bit 2's complement. Unit in 10pS.
0x29~0X2E	[47:0]	PHe_CALI	R		Phase error between 1PPS output and 1PPS input, after correction with user specified PD calibration value (see NPLL_PD_CAL1) and phase rebuilt bias. 48-bit 2's complement. Unit in 10pS.
0x2F~0x34	[47:0]	OUT_FFO	R		Output's normalized fractional frequency offset to calibrated MCLK frequency. 48-bit 2's complement. Unit in ppt ($=10^{-12}$)
0x35	[7:0]	NPLL_KICKUP	R/W	0	Write a non-zero value to this register to select 1PPS input pin and kickup NPLL. (1): Select pin IN1 as 1PPS input and kickup NPLL (2): Select pin IN2 as 1PPS input and kickup NPLL (3): Select pin IN3 as 1PPS input and kickup NPLL (4~255): Select no 1PPS input and kickup NPLL

NS2D04-1PPS Register Table continued

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
NPLL Continued					NPLL's run-time manual control 0: in normal operation 1: forced into manual LOS/Holdover 1: enable 2: disable 2,255: ~RSVI~
0x36	[7:0]	NPLL_RT_CTRL	R/W	0	
0x37	[7:0]	NPLL_FLL_PARA	R/W	0	NPLL FLL_LOCKING mode parameters bit[1:0] 2nd order low-pass filter's bandwidth index (0) 179 mHz (1) 90 mHz (2) 45 mHz (3) 22.5 mHz bit[7:2] peak-to-peak tolerance. - Fractional frequency change tolerance - Unit in ppb. The frequency tolerance feature has been changed from frequency offset between in-and-out to peak-to-peak output frequency change since FW rev 10.
0x38~0x39	[15:0]	NPLL_FLL_SOAKTIME	R/W	0	NPLL FLL_LOCKING mode soaking time. 15-bit. Unit in second. bit[14:0] soaking time, unit (second) bit[15:0] must be 0
0x3A	[7:0]	NPLL_PLL_PARA	R/W	0	NPLL PLL parameter bit[5:0] Loop bandwidth index in PLL_FAST_LOCKING mode bit[7:6] Damping factor Loop bandwidth in PLL_LOCKING / PLL_LOCKED mode: Loop bandwidth index must be no less than 10. Loop bandwidth = (1 / index), unit(Hz) Damping factor 0) 0.7 1) 1.4 2) 2.0 (3) 3.5
0x3B~0x3C	[15:0]	NPLL_RT_PLL_LBW_TARGET	R/W	0	NPLL PLL's target loop bandwidth index ▪ Target loop bandwidth index must be no less than the loop bandwidth index in PLL_FAST_LOCKING mode ▪ Loop bandwidth = (1 / index), unit(Hz) This is a run-time register.
0x3D~0x3E	[15:0]	NPLL_LEAKBUCK_THREASHOLD	R/W	0	NPLL PLL's leaking bucket threshold for all PLL_XXXX mode bit[15:0] phase error threshold. unit(nS)
0x3F~0x40	[15:0]	NPLL_LEAKBUCK_SIZE	R/W	0	NPLL PLL's leaking bucket size for all PLL_XXXX mode bit[15:0] bucket size
0x41~0x42	[15:0]	NPLL_RT_PHe_ReENTRY_TOL	R/W	0	NPLL's re-entry phase error tolerance. This tolerance is threshold of how to recover from LOS/HOLDOVER mode. bit[15:0] tolerance, unit(nS)
0x43~0x44	[15:0]	NPLL_RT_PHe_LOL_TOL	R/W	0	NPLL's LOL phase error tolerance. The tolerance is the threshold to trigger LOL alarm. bit[15:0] hard tolerance, unit(nS).
0x45	[7:0]	NPLL_CONFIG	R/W	0	NPLL's phase align configuration bit[0]: Phase aligned to 1PPS on XPLL: 1=YES, 0=NO bit[1]: Phase aligned to 1PPS on YPLL: 1=YES, 0=NO bit[3:2]: PLL_LBW_SHIFT_SPEED To specify the LBW shifting speed in PLL_LOCKING mode from LBW(FAST_LOCKING) to LBW (NORMAL) 0: normal 1: slower 2: slowest 3: faster bit[7:4]: ~RSVD~

NS2D04-1PPS Register Table continued

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
NPLL Continued					
0x46~4B	[47:0]	NPLL_RT_ALIGNED_OUT_FREQ	R/W	0	The frequency of output to align to 1PPS output. 17-bit. Unit in 8kHz. bit [16:0] n, freq = 8kHz x n bit [47:17] must be zero <ps.1> Setting the aligned output frequency to zero means 1PPS output pulse does not need to phase align to any other clock outputs <ps.2> This register used to be NPLL's configuration register and became NPLL's run-time register since firmware revision 0x03.
0x4C	[7:0]	NPLL_PBO_COMP_SPEED_MAX	R/W	0	The maximal phase shifting speed to compensate the previous PBO (phase build-out) phase error while entering PLL_FAST_LOCKING.) bit[7:6] band=0~3 bit[5:0] index=0~63 maximal shift speed = index x (16band) x (10 pS/S)
0x4D~0x4E	[15:0]	NPLL_RT_PD_CALI	R/W	0	User specified phase detector offset calibration, to cover 1PPS input's quantization error and cable latency delay. 16-bit 2's complement. - unit (10pS) This is a real-time register. This value will be applied to each 1PPS input phase offset reading. For each 1PPS input pulse, this value shall compliant to 1 uS **set-time** and 50 **uS hold-time**.
0x4F~0x54	[47:0]	NPLL_RT_MCLK_CALI	R/W	0	User specified MCLK frequency offset calibration. 28-bit 2's complement. Unit in (0.851495 ppt) bit [47:0] calibration offset, 2's complement unit (0.851495 ppt)
0x55~0x5F		~ RSVD			
XPLL1					
0x60~0x61	[12:0]	XPLL1_REF_FREQ_M	RW	1	NPLL synthesizes XPLL1's reference clock with frequency of (M *8kHz). 13-bit M value is set by this register. 1 <= M <= 5000
0x62		~ RSVD ~			
0x63~0x64	[14:0]	XPLL1_FB_DIV	RW	0	XPLL1 15-bit feedback divider value; Value 0 means disable
0x65	[0]	XPLL1_R0_SEL	RW	0	XPLL1 R0 selection, 0 Selection using Register XPLL1_R0_VALUE_L 1 Selection using Register XPLL1_R0_VALUE_S
0x66	[4:0]	XPLL1_R0_VALUE_S	RW	0	XPLL1 R0 value selection S. R0 is a combined resistor constituted of smaller resistors in series. Each bit controls one small resistor. Unit in ohm. Bit0 0: 0.4k, 1: 2.5k Bit1 0: 0.4k, 1: 5k Bit2 0: 0.4k, 1: 10k Bit3 0: 0.4k, 1: 20k Bit4 0: 0.4k, 1: 40k
0x67~0x68	[8:0]	XPLL1_R0_VALUE_L	RW	0	XPLL1 R0 value selection L. R0 is a combined resistor constituted of smaller resistors in series. Each bit controls one small resistor. Unit in ohm. Bit0 0: 1k, 1: 10k Bit1 0: 1k, 1: 20k Bit2 0: 1k, 1: 40k Bit3 0: 1k, 1: 80k Bit4 0: 1k, 1: 160k Bit5 0: 1k, 1: 320k Bit6 0: 1k, 1: 640k Bit7 0: 1k, 1: 1280k Bit8 0: 1k, 1: 2560k
0x69	[3:0]	XPLL1_R2	RW	0	XPLL1 R2 resistance = (160k ohm) / reg_value
0x6A~0x6B	[11:0]	XPLL1_CP_CURRENCY	RW	0	XPLL1 charge pump currency = 0.3125uA * reg_value
0x6C~0x6F		~ RSVD ~			

NS2D04-1PPS Register Table continued

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
XPLL2					
0x70	[2:0]	XPLL2_Pre_DIV	RW	0	The 3-bit divider value of the frequency pre-divider in front of XPLL2's PFD; Value 0 means disable
0x71	[6:0]	XPLL2_FB_DIV	RW	0	XPLL2 7-bit feedback divider value; Value 0 means disable
0x72	[0]	XPLL2_KVCO	RW	0	XPLL2 K_{VCO} 0 $K_{VCO} = K_{small}$ = 22k ppm/volt 1 $K_{VCO} = K_{large}$ = 33k ppm/volt
0x73	[0]	XPLL2_C0	RW	0	XPLL2 C0 value 0 100 pF 1 200 pF
0x74	[3:0]	XPLL2_R0	RW	0	XPLL2 R0 Value. Unit in ohm. 0:3k, 1:4.2k, 2:6k, 3:8.4k, 4:12k, 5:16.8k, 6:12k, 7:16.8k, 8:24k, 9:33.6k, 10:24k, 11:33.6k, 12:46.3k, 13:66k, 14:46.3k, 15:66k
0x75~0x76	[10:0]	XPLL2_CP_CURRENCY	RW	0	XPLL2 charge pump currency value; unit(1.25uA)
0x77~0x7F		~ RSVD ~			
YPLL1					
0x80~0x81	[12:0]	YPLL1_REF_FREQ_M	RW	1	NPLL synthesizes YPLL1's reference clock with frequency of (M *8kHz). 13-bit M value is set by this register. 1 <= M <= 5000
0x82		~ RSVD ~			
0x83~0x84	[14:0]	YPLL1_FB_DIV	RW	0	YPLL1 15-bit feedback divider value; Value 0 means disable
0x85	[0]	YPLL1_R0_SEL	RW	0	YPLL1 R0 selection, 0 Selection in Reg YPLL1_R0_VALUE_L 1 Selection in Reg YPLL1_R0_VALUE_S
0x86	[4:0]	YPLL1_R0_VALUE_S	RW	0	YPLL1 R0 value selection S. R0 is a combined resistor constituted of smaller resistors in series. Each bit controls one small resistor. Unit in ohm. Bit0 0: 0.4k, 1: 2.5k Bit1 0: 0.4k, 1: 5k Bit2 0: 0.4k, 1: 10k Bit3 0: 0.4k, 1: 20k Bit4 0: 0.4k, 1: 40k
0x87~0x88	[8:0]	YPLL1_R0_VALUE_L	RW	0	YPLL1 R0 value selection L. R0 is a combined resistor constituted of smaller resistors in series. Each bit controls one small resistor. Unit in ohm. Bit0 0: 1k, 1: 10k Bit1 0: 1k, 1: 20k Bit2 0: 1k, 1: 40k Bit3 0: 1k, 1: 80k Bit4 0: 1k, 1: 160k Bit5 0: 1k, 1: 320k Bit6 0: 1k, 1: 640k Bit7 0: 1k, 1: 1280k Bit8 0: 1k, 1: 2560k
0x89	[3:0]	YPLL1_R2	RW	0	YPLL1 R2 resistance = 160k ohm / reg_value
0x8A~0x8B	[11:0]	YPLL1_CP_CURRENCY	RW	0	YPLL1 charge pump currency = 0.3125uA * reg_value
0x8C~0x8F		~ RSVD ~			

NS2D04-1PPS Register Table continued

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
YPLL2					
0x90	[2:0]	YPLL2_Pre_DIV	RW	0	The 3-bit divider value of the frequency pre-divider in front of YPLL2's PFD; Value 0 means disable
0x91	[6:0]	YPLL2_FB	RW	0	YPLL2 7-bit feedback divider value; Value 0 means disable
0x92	[0]	YPLL2_KVCO	RW	0	YPLL2 K_{VCO} 0 $K_{VCO} = K_{small}$ = 22k ppm/volt 1 $K_{VCO} = K_{large}$ = 33k ppm/volt
0x93	[0]	YPLL2_C0	RW	0	YPLL2 C0 value 0 100 pF 1 200 pF
0x94	[3:0]	YPLL2_R0	RW	0	YPLL2 R0 Value. Unit in ohm 0: 3k, 1: 4.2k, 2: 6k, 3: 8.4k, 4:12k, 5: 16.8k, 6: 12k, 7: 16.8k, 8: 24k, 9: 33.6k, 10: 24k, 11: 33.6k , 12: 46.3k, 13: 66k, 14: 46.3k, 15: 66k
0x95~0x96	[10:0]	YPLL2_CP_CURRENCY	RW	0	YPLL2 charge pump currency value; unit(1.25uA)
0x97~0x9F		~ RSVD ~			
Alignment, Clock Distribution, and OUT11					
0xA0~0xA1	[11:0]	1PPS_PULSE_WIDTH	RW	10	1PPS output pulse width. Unit in uS.
0xA2	[3:0]	XPLL_ALIGN_PORT	RW	0	Select which output port sourced by XPLL to fine skew align to 1PPS output 0 skew alignment not required 1~8 Output 1~8 9~15 ~RSVD~
0xA3	[3:0]	YPLL_ALIGN_PORT	RW	0	Select which output port sourced by YPLL to fine skew align to 1PPS output Same as REG(XPLL_ALIGN_PORT)
0xA4	[0]	XPLL_OUT_SOURCE	RW	0	XPLL output source 0 XPLL1 1 XPLL2
0xA5	[0]	YPLL_OUT_SOURCE	RW	0	YPLL output source 0 YPLL1 1 YPLL2
0xA6	[2:0]	OUT_SOURCE_SEL	RW	0	Output 1~8 source selection, output can come from either XPLL or YPLL, the arrangement are as follows, 0,5,6,7 XPLL -> Output 1~8, YPLL -> none 1 XPLL -> Output 1~6, YPLL -> Output 7~8 2 XPLL -> Output 1~4, YPLL -> Output 5~8 3 XPLL -> Output 1~2, YPLL -> Output 3~8 4 XPLL -> none, YPLL -> Output 1~8
0xA7~0xA8	[13:0]	OUT11_SYNTH_FREQ			14-bit frequency value M for OUT11's synthesizer. Synthesizer Frequency = 8kHz * M, where 1,250 <= M <= 10,000, 0: disable, 1~1249: writing will be ignored
0xA9~0xAA	[15:0]	OUT11_SYNTH_FREQ_DIV			16-bit Value N for OUT11's synthesizer post divider Output Frequency = 8kHz *M / N, where 1 <= N <= 65535, 0: disable
0xAB~0xB0		~ RSVD ~			

NS2D04-1PPS Register Table continued

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
OUTPUT Transmitters					
0xB1		OUT1_TX_Mode	RW	0	Output0 transmitter mode, Bit[2:0] 0,6,7 power down the output driver 1 LVDS 2 LVPECL 3 LVCMOS, P on, N off 4 LVCMOS, P off, N on 5 LVCMOS, P on, N on When transmitter is in LVCMOS mode, bit[4:3] are to program the clock edge of each output pin Bit[3] for pin-P clock output 0: clock on the rising-edge 1: clock on the falling-edge Bit[4] for pin-N clock output 0: clock on the rising-edge 1: clock on the falling-edge.
0xB2	[4:0]	OUT2_TX_Mode	RW	0	Output2 transmitter mode; Same as Output1 Transmitter Mode
0xB3	[4:0]	OUT3_TX_Mode	RW	0	Output3 transmitter mode; Same as Output1 Transmitter Mode
0xB4	[4:0]	OUT4_TX_Mode	RW	0	Output4 transmitter mode; Same as Output1 Transmitter Mode
0xB5	[4:0]	OUT5_TX_Mode	RW	0	Output5 transmitter mode; Same as Output1 Transmitter Mode
0xB6	[4:0]	OUT6_TX_Mode	RW	0	Output6 transmitter mode; Same as Output1 Transmitter Mode
0xB7	[4:0]	OUT7_TX_Mode	RW	0	Output7 transmitter mode; Same as Output1 Transmitter Mode
0xB8	[4:0]	OUT8_TX_Mode	RW	0	Output8 transmitter mode; Same as Output1 Transmitter Mode
0xB9	~ RSVD ~				
OUTPUT Post Dividers					
0xC0~0xC2	[19:0]	OUT1_DIV	RW	0	20-bit OUTPUT1 divider value; Value 0 means divider disable; Value 1 means bypassing the divider
0xC3~0xC5	[19:0]	OUT2_DIV	RW	0	20-bit OUTPUT2 divider value; Value 0 means divider disable
0xC6~0xC8	[19:0]	OUT3_DIV	RW	0	20-bit OUTPUT3 divider value; Value 0 means divider disable; Value 1 means bypassing the divider
0xC9~0xCB	[19:0]	OUT4_DIV	RW	0	20-bit OUTPUT4 divider value; Value 0 means divider disable
0xCC~0xCE	[19:0]	OUT5_DIV	RW	0	20-bit OUTPUT5 divider value; Value 0 means divider disable
0xCF~0xD1	[19:0]	OUT6_DIV	RW	0	20-bit OUTPUT6 divider value; Value 0 means divider disable; Value 1 means bypassing the divider
0xD2~0xD4	[19:0]	OUT7_DIV	RW	0	20-bit OUTPUT7 divider value; Value 0 means divider disable
0xD5~0xD7	[19:0]	OUT8_DIV	RW	0	20-bit OUTPUT8 divider value; Value 0 means divider disable; Value 1 means bypassing the divider
0xD8~0xEF		~ RSVD ~			

NS2D04-1PPS Register Table continued

ADDR	BITS	NAME	I/O	DEFAULT	DESCRIPTION
EEPROM, Loader, and Soft Reset					
0xF0	[0]	EE_STS	R		EEPROM status 0: not ready 1: ready
0xF1~0xF2	[15:0]	EE_PAGE_IDX	RW	0	9-bit EEPROM page index, (1 page = 64-byte) bit[15] must be 0 bit[14:6] page index bit[6:9] must be 0b000000
0xF3	[7:0]	EE_FIFO	RW	0	8-bit EEPROM read/write FIFO port to 1 page (= 64-byte) FIFO buffer
0xF4	[1:0]	EE_CMD	RW	0	EEPROM command 0: reset FIFO pointer 1: load 1-page data from EEPROM to 64-byte FIFO buffer 2: burn 1-page data from FIFO buffer to EEPROM 3: ~ RSVD ~
0xF5~0xF6		~ RSVD ~			
0xF8	[7:0]	SOFT_RESET	W		To soft-reset this IC by writing 0xA5 into this register
0xF8	[0]	LOAD_STS	R		OTP/EEPROM Loading status 0: not complete 1: complete
0xF9	[1:0]	LOAD_CRC_STS	R		Loader Checksum status bit[0]: CONFIG 0:FAILED, 1:PASSED bit[1]: CODE 0:FAILED, 1:PASSED
0xFA~0xFF		~ RSVD ~			

Register Programming Sequence Recommendation

For all NS2D00/04's registers to be programmed, a programming sequency is recommended here. Most of the programmable registers are related to each other so the programming sequence matters. All those registers could be separated into 7 programming sections. We recommend to program those registers following our programming section order, from section 1 to section 7. Inside the same programming section, the register programming order has no restriction.

Section [1]

- XPLL_OUT_SOURCE
- YPLL_OUT_SOURCE
- OUT_SOURCE_SEL

Section [2]

- OUT1~8_TX_Mode
- OUT1~8_DIV

Section [3]

- XPLL_ALIGN_PORT
- YPLL_ALIGN_PORT

Section [4]

- XPLL1/YPLL1_REF_FREQ_M
- XPLL1/YPLL1_FB_DIV
- XPLL1/YPLL1_R0_SEL
- XPLL1/YPLL1_R0_VALUE_S
- XPLL1/YPLL1_R0_VALUE_L
- XPLL1/YPLL1_R2
- XPLL1/YPLL1_CP_CURRENCY
- XPLL2/YPLL2_Pre_DIV
- XPLL2/YPLL2_FB_DIV
- XPLL2/YPLL2_KVCO
- XPLL2/YPLL2_C0
- XPLL2/YPLL2_R0
- XPLL2/YPLL2_CP_CURRENCY

The programming order of the following programmable registers doesn't matter.

- 1PPS_PULSE_WIDTH
- OUT11_SYNTH_FREQ
- OUT11_POST_DIV
- OUT0_TX_Mode ….. (if exists)
- OUT9_TX_Mode ….. (if exists)
- NPLL_RT_CTRL
- NPLL_RT_PLL_LBW_IDX_TARGET
- NPLL_RT_PHe_ReENTRY_TOLERANCE
- NPLL_RT_PHe_LOL_TOLERANCE
- NPLL_RT_PD_CALI
- NPLL_RT_MCLK_CALI
- NPLL_RT_ALIGNED_OUT_FREQ

Section [5]

- XPLL_Mode
- YPLL_Mode

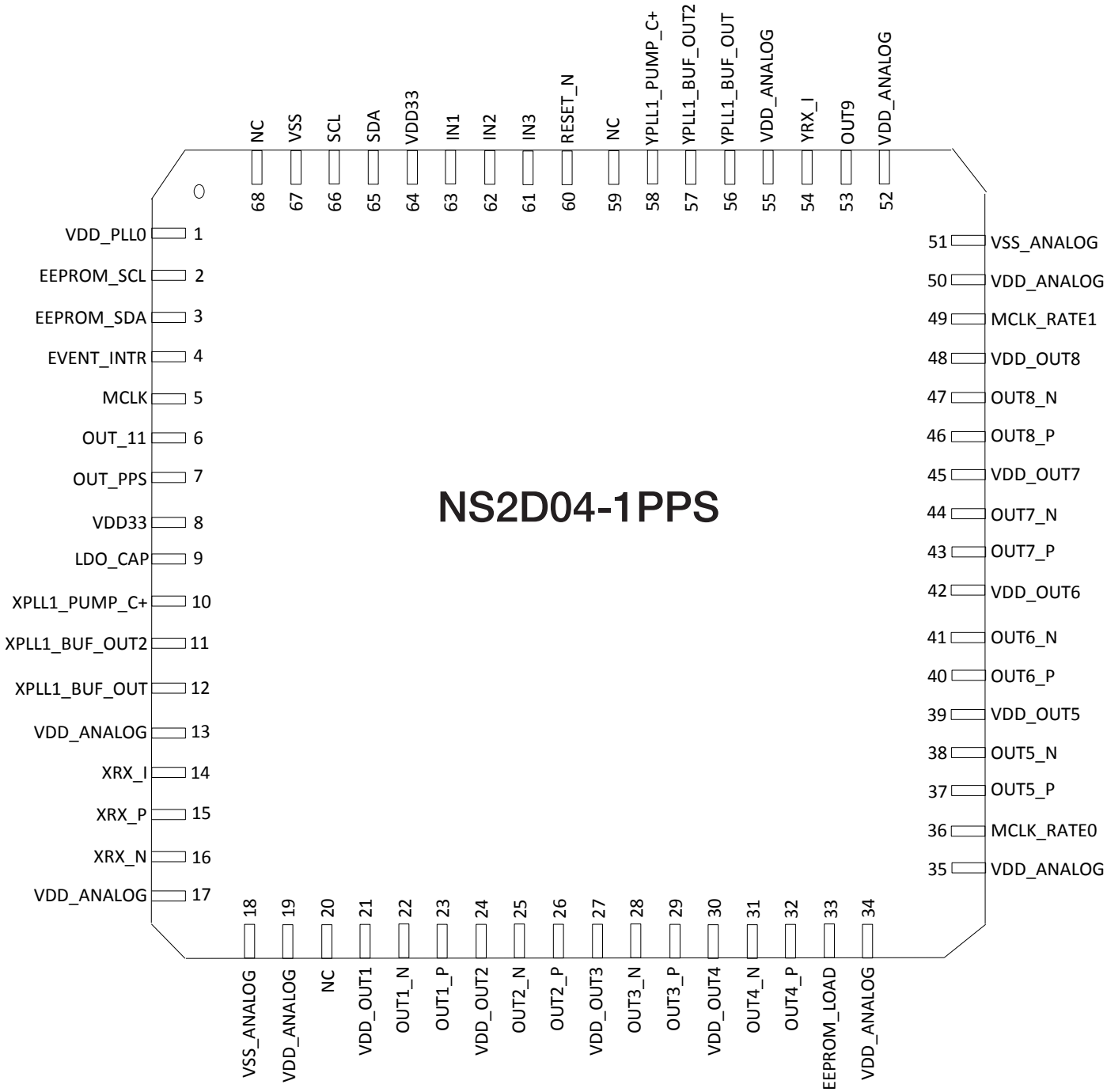
Section [6]

- NPLL_FLL_PARA
- NPLL_FLL_SOAKTIME_S
- NPLL_PLL_PARA
- NPLL_RT_PLL_LBW_IDX_TARGET
- NPLL_LEAKBUCK_THRESHOLD
- NPLL_LEAKBUCK_SIZE
- NPLL_RT_PHe_ReENTRY_TOLERANCE
- NPLL_RT_PHe_LOL_TOLERANCE
- NPLL_CONFIG
- NPLL_RT_ALIGNED_OUT_FREQ
- NPLL_PBO_COMP_SPEED_MAX

Section [7]

- NPLL_KICKUP

NS2D04-1PPS Pin Assignments (Top View)



Pin Connection Recommendations

- VDD Pins and Decoupling: all VDD pins must always be connected.
- Unused Clock Outputs: leave unused clock outputs floating and powered down.
- Unused XRX and YRX input pins can be left floating and powered down.

NS2D04-1PPS Pin Description

Pin No.	Pin Name	I/O	Description
1	VDD_PLL0	Power	3.3V Digital Power input
2	EEPROM_SCL	O	Serial Clock Output
3	EEPROM_SDA	I/O	Serial Data
4	EVENT_INTR	O	
5	MCLCK	I	Master Clock input
6	OUT_11	O	3.3V LVCMOS Output
7	OUT_PPS	O	1PPS Output Generator
8	VDD33	Power	3.3V digital power input
9	LDO_CAP		Connect internal LDO to external MLCC capacitor to GND (~1 uF) *Note: keep trace very short between IC and Cap*
10	XPLL1_PUMP_C+		Connect to APLL's external filter +
11	XPLL1_BUF_OUT2		Connect to VCXO voltage control pin (optional connecting to cap)
12	XPLL1_BUF_OUT		Connect to VCXO voltage control pin (optional connecting to cap)
13	VDD_ ANALOG	Power	3.3V Analog power input)
14	XRX_1	I	Accept XO or VCXO's 3.3V LVCMOS clock output
15	XRX_P	I	Accept XO or VCXO's 3.3V Differential (P) clock output
16	XRX_N	I	Accept XO or VCXO's 3.3V Differential (N)clock output
17	VDD_ANALOG	Power	3.3V Analog power input
18	VSS_XPLL2	Power	Analog ground
19	VDD_ANALOG	Power	3.3V Analog power input
20	NC		
21	VDD_OUT1	Power	3.3V Analog power input
22	OUT1_N	O	Differential output 0 negative (LVPECL/LVDS) or LVCMOS
23	OUT1_P	O	Differential output 0 positive (LVPECL/LVDS) or LVCMOS
24	VDD_OUT2	Power	3.3V Analog power input
25	OUT2_N	O	Differential output 1 negative (LVPECL/LVDS) or LVCMOS
26	OUT2_P	O	Differential output 1 positive (LVPECL/LVDS) or LVCMOS
27	VDD_OUT3	Power	3.3V Analog power input
28	OUT3_N	O	Differential output 2 negative (LVPECL/LVDS) or LVCMOS
29	OUT3_P	O	Differential output 2 positive (LVPECL/LVDS) or LVCMOS
30	VDD_OUT4	Power	3.3V Analog power input
31	OUT4_N	O	Differential output 3 negative (LVPECL/LVDS) or LVCMOS
32	OUT4_P	O	Differential output 3 positive (LVPECL/LVDS) or LVCMOS
33	EEPROM_LOAD	I	Reset pin
34	VDD_ANALOG	Power	3.3V Analog power input
35	VDD_ANALOG	Power	3.3V Analog power input
36	MCLCK_RATE0		Master clock rate Set pin
37	OUT5_P	O	Differential output 4 positive (LVPECL/LVDS) or LVCMOS
38	OUT5_N	O	Differential output 4 negative (LVPECL/LVDS) or LVCMOS
39	VDD_OUT5	Power	3.3V Analog power input
40	OUT6_P	O	Differential output 5 positive (LVPECL/LVDS) or LVCMOS

NS2D04-1PPS Pin Description continued

Pin No.	Pin Name	I/O	Description
41	OUT6_N	O	Differential output 5 negative (LVPECL/LVDS) or LVCMOS
42	VDD_OUT6	Power	3.3V Analog power input
43	OUT7_P	O	Differential output 6 positive (LVPECL/LVDS) or LVCMOS
44	OUT7_N	O	Differential output 6 negative (LVPECL/LVDS) or LVCMOS
45	VDD_OUT7	Power	3.3V Analog power input
46	OUT8_P	O	Differential output 7 positive (LVPECL/LVDS) or LVCMOS
47	OUT8_N	O	Differential output 7 negative (LVPECL/LVDS) or LVCMOS
48	VDD_OUT8	Power	3.3V Analog power input
49	MCLK_RATE1		Master clock rate Set pin
50	VDD_ANALOG	Power	3.3V Analog power input
51	VSS_ ANALOG	Power	Analog ground
52	VDD_ANALOG	Power	3.3V Analog power input
53	OUT_9	O	3.3V CMOS clock output
54	YRX_1	I	Accept VCXO's 3.3V clock output
55	VDD_ANALOG	Power	3.3V Analog power input
56	YPLL1_BUF_OUT		Connect to VCXO voltage control pin (optional connecting to cap)
57	YPLL1_BUF_OUT2		Connect to VCXO voltage control pin (optional connecting to cap)
58	YPLL1_PUMP_C+		Connect to APLL's external filter +
59	NC		
60	RESET_N	I	Reset pin. Active Low, internally pulled up high
61	IN3	I	Reference Input 1PPS
62	IN2	I	Reference Input 1PPS
63	IN1	I	Reference Input 1PPS
64	VDD33	Power	3.3V Digital Power Input
65	I2C_SDA	I	I2C Serial Data
66	I2C_SCL	I	I2C Serial Clock
67	VSS	Power	Digital Ground
68	NC		

Notes on Pin Description

RESET_N

Pin RESET_N is an I/O input pin used to initiate a “hard” reset to the IC. The RESET_N pin is internally “pulled-high”. Driving this pin “Low” for at least 1uS and releasing it, or driving it “High” again will reset the device. The IC will be ready to access through the control bus interface in 10 mS after the reset operation.

In addition to the RESET_N hardware pin reset function, a SOFT_RESET reboot option exists in the IC’s internal design. The register “SOFT_RESET” at 0 xA5 is a write-only register. Similar to the hard reset, once the register is written to, the IC’s registers will be ready to access through the control bus interface after 10mS.

Both the hard reset and the soft reset will cause the IC to reboot. The reboot procedure will first reload the content from the internal OTP. If the EEPROM_LOAD pin is tied “high”, an external EEPROM’s content will be loaded into the IC after the OTP content is loaded. Only the hard reset procedure will check the MCLK_RATE0 and MCLK_RATE1 to determine the clock frequency of the MCLK input.

This IC has a built-in power-on-reset (POR) circuit. However, a hard reset may need to be initiated if the supplied voltage to the IC has a very slow rising rate.

EEPROM_LOAD

EEPROM OPERATION: This IC supports the use of an external EEPROM to load firmware or default values of all read/write registers. This function is intended primarily to provide the ability for “field upgrade” flexibility to update firmware (Code+Data). Using an external EEPROM may also be considered for loading the default values of the read/write registers in preference to using the OTP memory. However, EEPROM content cannot be used to change the default values of read-only registers. CRC16 checksum protection is supported.

EEPROM BOOTING: The IC will always boot from the internal OTP content first. If the pin EEPROM_LOAD is tied “HIGH”, the IC will continue to download content from the EEPROM to override the OTP’s content during the boot-up stage. This procedure will be triggered after both a power cycle and a reset procedure (Hard or Soft).

EEPROM CONNECTION: This IC has an I2C master control dedicated to read/write data from a specific I2C EEPROM. The ATMEL AT24C256C (256-kbit I2C EEPROM IC) is required for use with this IC. For connection:

EEPROM’s I2C address ended with 0b000
- Ties pin A0, A1, A2 to ground

Disable write protection
- Ties pin WP to ground

Connect to this IC
- Tie pin SCL to this IC’s pin EEPROM_SCL
- Tie pin SDA to this IC’s pin EEPROM_SDA
- Data rate will be 1MHz (if traces are too long, some termination may be required)

EEPROM UPDATE OPERATION FROM USERS: This IC supports I2C bus interface as a control interface. This means the user can read/write content from/to the external EEPROM from this IC.

The EEPROM operations registers on this IC are:
- REG (EE_STS)
- REG (EE_PAGE_IDX)
- REG (EE_FIFO)
- REG (EE_CMD)

EEPROM content image
- Image size = 18,048 bytes
- Image content will be provided by manufacturer
- Each EEPROM image will be presented by an 18,048-byte long binary file
- Image integrity is protected by industry-grad CRC16 checksum

EEPROM Read/Write Operation
- Both read/write operation is in 64-byte page orientation
- The 18,048-byte binary image will be separated into 282 64-byte pages, indexed from 0 to 281

Page WRITE operation example:
- Wait until EE_STS indicates it is “ready”
- Setup the corresponding page index
- Issue FIFO pointer reset command
- Issue FIFO-read-from-EEPROM command
- Wait until EE_STS indicates it is ready
- Read the 64 byte page content from the FIFO port, in the order from LSB byte
- After updating the EEPROM content, read them back to ensure no corrupt data was generated during the read/write operation.

Notes on Pin Description continued

EEPROM_LOAD continued

Page READ operation example:

- Wait until EE_STS indicates IC is “ready”
- Setup the corresponding page index
- Issue FIFO pointer reset command
- Issue FIFO-read-from-EEPROM command
- Wait until EE_STS indicates IC is ready
- Read the 64 byte page content from the FIFO port, in the order from LSB to MSB byte
- After updating the EEPROM content, read them back to ensure no corrupt data was generated during the read/write operation.

CONTROL -BUS OPERATION

The control bus type of this IC uses a standard I2C interface. The I2 C interface has the advantage of requiring only two control pins and is a de facto standard throughout the I2C industry. The I2C port consists of a serial data line (SDA) and a serial clock line (SCL). In an I2C bus system, the NS2D04 is connected to the serial bus (data bus SDA and clock bus SCL) as a slave device; that is, no clock is generated by the NS2D04. The NS2D04 uses direct 8-bit memory addressing.

Users can read/write registers through this control bus. The I2C slave controller does not support multi-master operation. Supporting clock rate is up to 1MHz.

The fixed I2C address is: Slave address = 0b101.0001

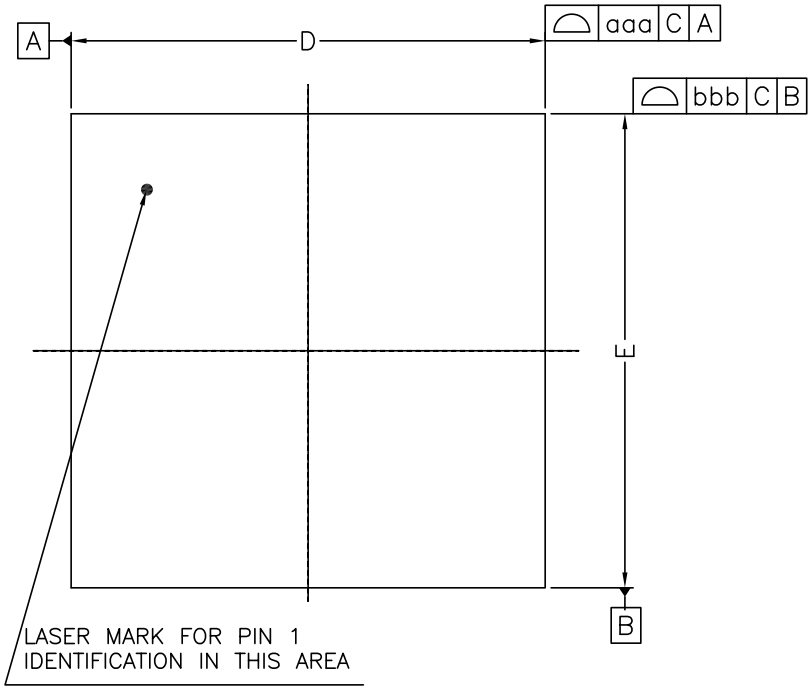
I2C frame and data transfer format-

This IC supports a 7-bit I2C address (slave address = 0b101.0001). The format is MSB-bit leading. This format uses only one byte for the 8-bit RAM/REG address. When read/write in burst mode (i.e. more than one data byte in an I2C frame), the RAM/REG address will be increased by one automatically for each data byte.

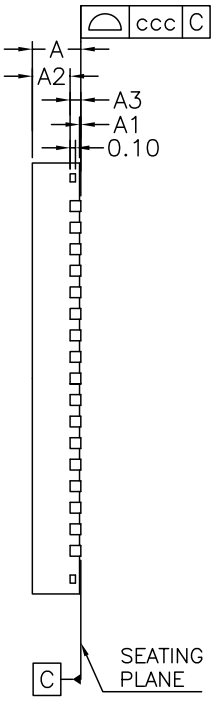
Multi-Byte Register Operation-

This IC has many registers. Some of these registers are a single byte and some are a multi-byte format. A Register's address is in unit of byte. For each multi-byte register, it forms in LSB (least significant byte) first order. The LSB byte shall have a lower address. When read/write to a multi-byte register, you must always access in the order from LSB byte to MSB byte. You should not interrupt a multi-byte register read/write with other bus operations. The writing to a multi-byte register will take effect when you are writing its MSB byte.

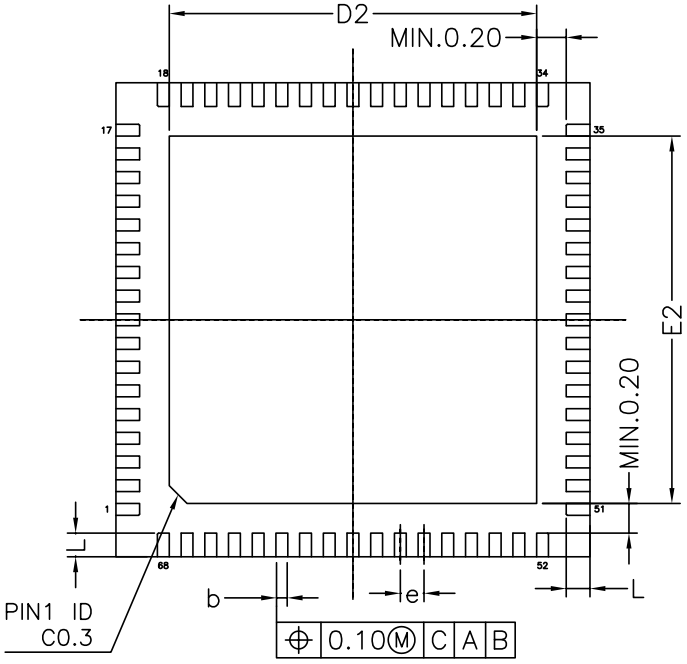
8 x 8 mm 68 pin QFN Mechanical Outline



TOP VIEW



SIDE VIEW



BOTTOM VIEW

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.00	0.001	0.002
A2	---	0.65	0.67	---	0.026	0.026
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	7.90	8.00	8.05	0.311	0.315	0.317
D2	6.10	6.20	6.30	0.240	0.244	0.248
E	7.90	8.00	8.05	0.311	0.315	0.317
E2	6.10	6.20	6.30	0.240	0.244	0.248
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

APPENDIX 1

Layout Recommendations

The printed circuit board that houses the NS2D04-1PPS should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should be joined in only one place. If the NS2D04-1PPS is the only device requiring an AGND-to-DGND connection, then the ground planes should be connected at the AGND and DGND pins of the NS2D04-1PPS. If the NS2D04-1PPS is in a system where multiple devices require AGND-to-DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the NS2D04-1PPS.

Avoid running digital lines under the device because these couple noise onto the die. The analog ground plane should run under the NS2D04-1PPS to avoid noise coupling. The power supply lines to the NS2D04-1PPS should use as large a track as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other, reducing the effects of feed-through. A micro-strip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the other side.

Good decoupling is important. The analog and digital supplies to the NS2D04-1PPS are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND, respectively, with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors. To achieve the best from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply is used to drive both the AVDD and DVDD of the NS2D04-1PPS, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pin of the NS2D04-1PPS and AGND and the recommended digital supply decoupling capacitors between the DVDD pin and DGND.

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Ordering Information

NS2D04

Part Number

Revision History

Revision	Date	Note
00	03/23/22	New issue to update NS2D04 new firmware
01	04/28/22	Updated Pin Descriptions BUF_OUT and BUF_OUT 2
02	05/26/22	Updated Registries 0x65 and 0x85
03	10/31/23	Updated registers 0x37, 0xB0, and 0xB9