EH320-TFC-CC-OPL
1PPS Time to Frequency Converter Module

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DATA SHEET

RoHS COMPLIANT

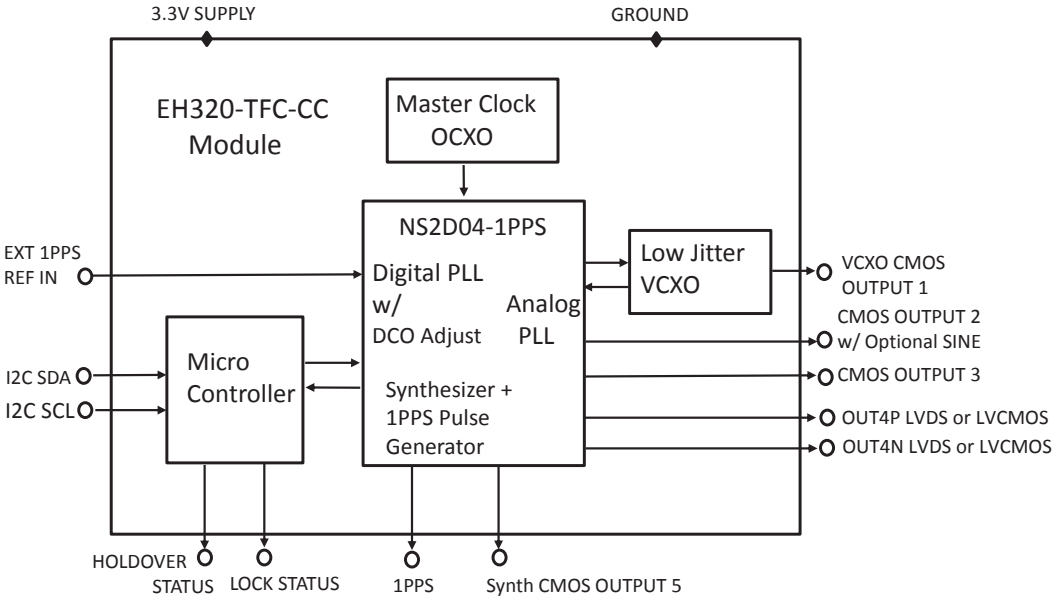
Overview

The EH320-TFC Series is a highly integrated time and frequency synchronizing module. This design implementation is dedicated for use in applications which specifically require locking to an incoming 1PPS reference signal. This high precision phase and frequency synchronization solution also integrates “any frequency” clock signal generation and frequency translation. This product can be used to support a high-stability frequency reference for use in wireless systems, IEEE 1588v2, and applications employing a 1PPS frequency source for high precision, long term time and frequency generation. The -CC module option includes an on board OCXO that is further compensated for thermal stability to less than ±0.5ppb, which provides the system’s master clock for disciplining the internal DPLL and supports the holdover performance when the 1PPS incoming reference signal is lost. The EH320-TFC-CC module outputs a 1PPS signal and a digitally synthesized 3.3V LVCMOS clock output at frequencies from 152Hz to 80 MHz. In addition, the module can generate up to 5 additional clean clock outputs at a variety of frequencies from 750MHz to <1KHz. The generated frequency outputs are both phase and frequency locked to the incoming 1PPS reference signal.

Features

- Accepts 1 PPS Reference input
- Locked, Holdover indication
- 1 PPS & NCO Frequency Output
- “Any Frequency” Generation from 152 Hz to 80MHz
- 1PPS Auto-detect
- Automatic entry into holdover
- 3.3VDC Supply Voltage
- Five Clean low phase noise clock outputs
- One Differential LVDS or LVPECL output to 750MHz
- CC Option for Sub ±0.5 ppb holdover performance
- OCXO Master Clock
- Phase and Frequency locked outputs
- -40°C to 85°C operating temperature range
- OEM SM footprint 25 x 22 mm
- RoHS Compliant ✓RoHS

Figure 1: EH320-TFC-CC Functional Block Diagram



Bulletin	SG202
Revision	00
Date	30 Sept 2020

1 INTRODUCTION

The EH320-TFC-CC is a small OEM surface mount timing module specifically designed for use in synchronization and timing applications. This module incorporates Connor-Winfield's advanced NS2D04 synchronizing ASIC which integrates a digital phase lock loop system with an analog phase lock loop system and multiple output transmitters to allow the user to discipline an external 1PPS signal and generate multiple output clocks phase locked and aligned to the incoming 1PPS reference.

The digital PLL system design supports multiple bandwidth settings used for disciplining the incoming 1PPS signal. The DPLL system in the EH320-TFC-CC is supported by a master clock which is derived from a high precision/low ADEV OCXO that is further internally compensated for thermal instability to achieve sub 1ppb thermal frequency stability while the module is in free run and holdover. Due to the ultra low ADEV performance of the module's master clock, the DPLL bandwidth in the EH320-TFC-CC is set to <1mHz.

The EH320-TFC-CC module auto-detects a valid incoming 3.3V 1PPS reference signal. When a valid 1PPS signal is present, the module has a three stage locking process starting with a frequency locking stage, followed by a fast phase locking stage before achieving full phase locking. The module is allowed to soak in a fast locking stage for a period of time while the OCXO has time to settle. After the frequency locking phase is complete, the 1PPS alignment process moves to within the closest period of the lowest common output frequency. A phase build-out process then adjusts and pulls the remaining phase offset alignment until fully aligned. For phase alignment to take place, frequencies must be divisible by 8kHz.

The DPLL block implements a digital synthesizer that generates an outgoing 1PPS, a variable frequency synthesized clock made available to the user in Output 5, and a synthesized clock that is sent to the Analog PLL sys-tem within the ASIC. Using a low jitter internal VCXO, the module generates multiple clock outputs at frequencies integer related to the VCXO frequency. Output 1 is the frequency of the VCXO used in the module. Output 2 and 3 are both 3.3V CMOS outputs and output 4 P/N can be configured as a differential signal (LVDS or LVPECL) or two CMOS outputs at the same frequency. Outputs 1 through 4 are derived from the frequency of the VCXO, directly divided at the output transmitter port. If frequencies higher than 125MHz are required, a secondary APLL block can be employed to integer divide outputs from a high frequency VCO in the range of 1.2 GHz to 1.46 GHz. If this secondary APLL is used, all outputs must be generated from this system, except for output 1 which always is derived from and is the same as the VCXO frequency. Except for output 1 and output 5, the output ports each have 20-bit dividers that can be used from either the VCXO frequency using the first PLL option or the VCO frequency if the second PLL block is used. Output 5 is a 3.3V CMOS output than can be programmed to any 8kHz divisible frequency from 10M to 80MHz and then further divided with an integer post divider with a 16 bit capability.

The EH320-TFC-CC incorporates a micro controller that moderates the internal ASIC, setting the registers and monitors operations. The module is programmed at the factory but some system commands may be available for changing some registers. The module is intended to be defined and provided to the user as a complete system capable of operating with no user input required.

The EH320-TFC-CC is RoHS and REACH compliant. It's highly integrated architecture is packaged in a small 22x25mm surface mount footprint allowing for easy integration into host systems.

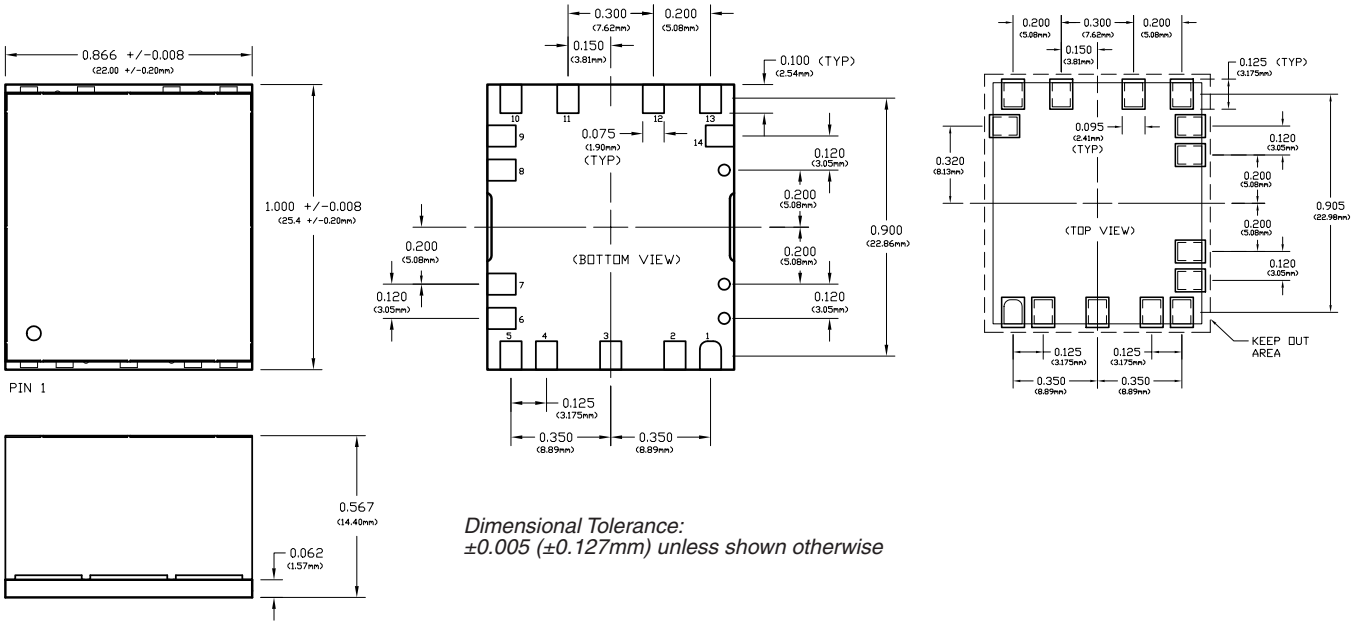
For more detailed information on the operation of the internal system ASIC NS2D04, see the following data sheet. ***http://www.conwin.com/datasheets/tm/tm138.pdf***

2 PHYSICAL CHARACTERISTICS

The EH320-TFC-CC is a multi-chip module (MCM) built on an FR4 fiberglass 22x25mm PCB. The general arrangement of the EH320-TFC-CC is shown in the diagram below.

Mechanical Drawing

Suggested Pad Layout



Dimensional Tolerance:
±0.005 (±0.127mm) unless shown otherwise

Figure 2 EH320-TFC-CC Mechanical Drawing and Suggested Pad Layout

2.1 Pin Functions

Pin	Function	Pin	Function	Pin	Function
1	FREQ_OUT2	6	LOCKED	11	I2C SCL
2	1 PPS_IN	7	HOLDOVER	12	I2C SDA
3	FREQ_OUT3	8	FREQ_OUT4P	13	GND
4	1PPS_OUT	9	FREQ_OUT4N	14	FREQ_OUT5 Variable
5	VCC_3V3	10	FREQ_OUT1 VCXO		

EH320-TFC-CC-DK1 Configuration

VCXO Frequency	Output 1 VCXO	Output 2	Output 3	Output 4P/4N	Output 5 Variable
10 MHz	10 MHz LVCMOS	10 MHz Sinewave	10 MHz LVCMOS	N/C	N/C

3 PERFORMANCE COMPARISON

The EH320-TFC model series allows for a choice of master clock options which dictate the bandwidth setting chosen to optimize performance. The -CC option allows for loop bandwidth settings of 1 mHz or less due to its master clock ultra-low ADEV performance.

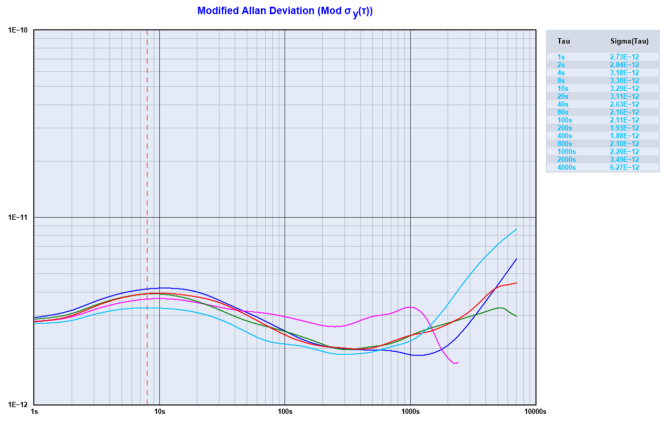


Figure 3 EH320-TFC-CC (in Free run) Modified Allan Deviation Graph

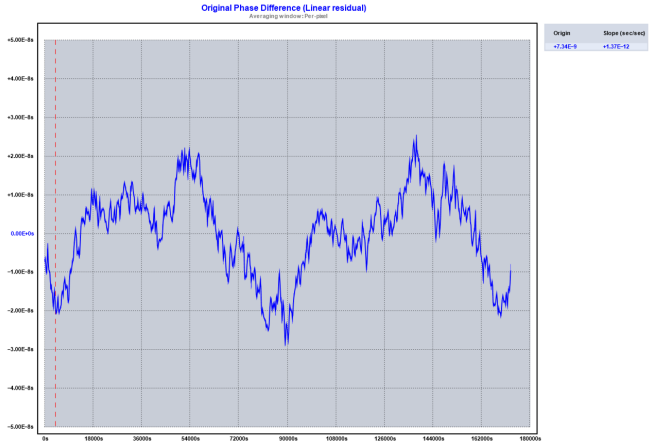


Figure 4 EH320-TFC-CC Phase Tracking in lock mode

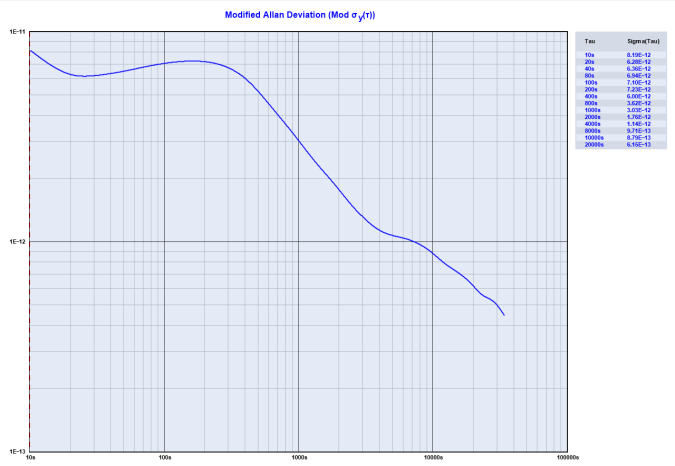


Figure 5 EH320-TFC-CC (in lock mode) Modified Allan Deviation Graph

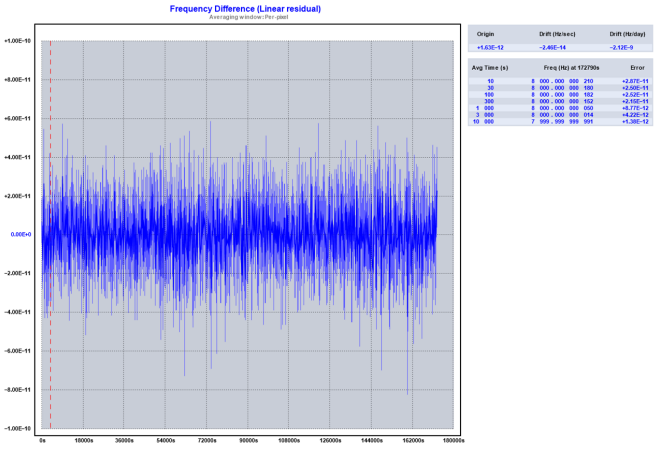


Figure 6 EH320-TFC-CC Frequency Difference in lock mode

4 SIGNAL DESCRIPTION

The signals on the EH320-TFC-CC are described in the table below.

4.1 Power Signals

VCC_3V3	Type: Power	Direction: Input	Pin: 5
	The Supply Input. This 3.3V ± 10% input supplies power to the module		
GND	Type: Power	Direction: Input/Output	Pin: 13
	The Input Ground. This is the return path for the vcc_3V3 supply and the ground for the module.		

4.2 I/O Signals

TX[0]	Type: I/O	Direction: Output	Pin: 11
	I2c SCL PIN		
RX[0]	Type: I/O	Direction: Input	Pin: 12
	I2c SDA PIN		
HOLDOVER	Type: I/O	Direction: Output	Pin: 7
	Standard software builds use this signal to indicate Holdover status. High indicates holdover mode. This signal has a 3.3V CMOS drive.		
LOCKED	Type: I/O	Direction: Output	Pin: 6
	Standard software builds use this signal to indicate LOCK status. High indicates locked to 1pps. This signal has a 3.3V CMOS drive.		
FREQ_OUT1 VCXO	Type: I/O	Direction: Output	Pin: 10
	Primary output of the module which is a pass through of the frequency of the VCXO internal to the module.		
FREQ_OUT2	Type: I/O	Direction: Output	Pin: 1
	Second output from the module that can be provided as either 3.3V LVCMOS or 3.3V Sinewave.		
FREQ_OUT3	Type: I/O	Direction: Output	Pin: 3
	Third output from the module 3.3V LVCMOS.		
FREQ_OUT4P/N	Type: I/O	Direction: Output	Pin: 8, 9
	Fourth output from the module that can be provided as either 3.3V LVDS, 3.3V LVPECL or 2 x 3.3V LVCMOS.		
1 PPS_IN	Type: I/O	Direction: Input	Pin: 2
	The 1 Pulse-Per-Second Reference Input Signal. This is normally as a 1 pulse aligned with GPS time, generated by an external GPS/GNSS source.		

4.1 I/O Signals cont'd

1 PPS_OUT	Type: I/O	Direction: Output	Pin: 4

The 1 Pulse-Per-Second Signal.
This is normally as a 1 pulse aligned with incoming 1PPS_IN signal.

FREQ_OUT5 Variable	Type: I/O	Direction: Output	Pin: 14

Frequency Output that defaults to 10 MHz and is user configurable. The output is enabled on power-up and is steered by the incoming 1PPS signal. This clock output is a 3.3V LVCMOS single ended signal generated by the internal NCO with output frequency values achievable from 152Hz to 80MHz.
Internally, the frequency output is a value determined by two separate register settings. An initial value of M is used to multiply 8kHz to a frequency in the range between 10MHz and 80MHz. Once the M value is determined, a 16-bit post divider can be employed to generate a set of lower rate frequencies by choosing an N value which divides the base frequency by that number. V alid M values are integer numbers >= 1250 and <=10,000.V alid N values are integer numbers =>1 and <= 65536. A "0" value for M will disable the output while a "0" value for N will disable the post divider.

To simplify the process for the user to set the output frequency, a command system is in place to for changing the frequency of the output on the fly. The format of the command sentence that sets the frequency of the NCO and the output divider is: $PRTHS, FREQ, XXXXXXXX,YY
Form
$PRTHS,FREQ,<freq>,<divisor>
where
<freq >: In range of 10 MHz to 80 MHz, 8 kHz steps
<divisor> : In range of 0 to 65535, 0=Off

X is the frequency of the NCO and YY is the divide ratio of the output divider. For example if you sent $PRTHS, FREQ, 10000000, 10 The output frequency would be 1 MHz. The response from the module would be $PRTHR, FREQ, 10000000, 10*CS where "CS" is a checksum.
If the frequency or divider is out of range, the module responds with $POLYD,FREQ,BADPARAMS*15. In the case where an out of range parameter setting is used, the module will set the output to the nearest legal value.

Example: Set with incorrect or out-of-range parameters
Sent $PRTHS,FREQ,307200,1
Response $POLYD,FREQ,BADPARAMS*15

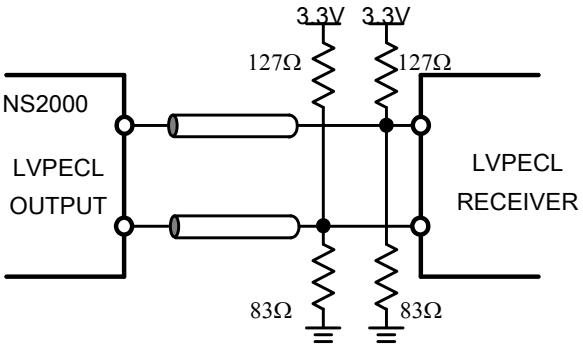
Set with acceptable parameters
Sent $PRTHS,FREQ,10000000,1
Response $PRTHR,FREQ,10000000,1*50

Startup
$POLYD,EH320-TFC,17:45:38,Aug-14-2019*5D
$PRTHR,FREQ,40000000,4*50

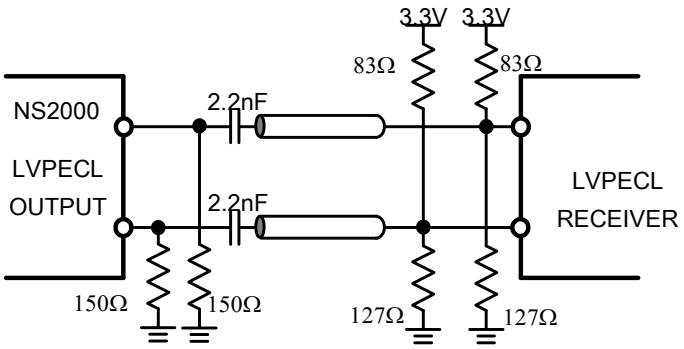
Query Current
Sent $PRTHQ,FREQ
Response $PRTHR,FREQ,40000000,4*50

NOTE: Phase alignment between the 1PPS incoming reference and the frequency output is possible only if the synthesized output frequency is integer related to 8kHz. All frequencies generated by values of only M will be phased aligned with the incoming 1PPS signal. However, using the 16 bit post divider, only N values chosen that result in an output frequency that has an integer relationship with 8kHz will be phase aligned to the incoming 1PPS signal.

LVPECL Suggested Termination



DC-Coupled LVPECL Termination



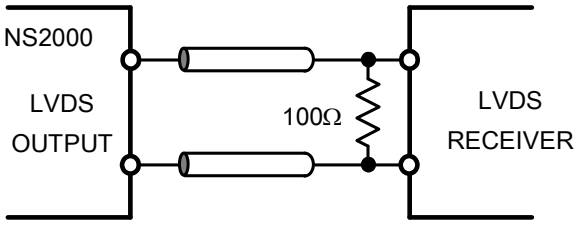
AC-Coupled LVPECL Termination

LVPECL Current Consumption

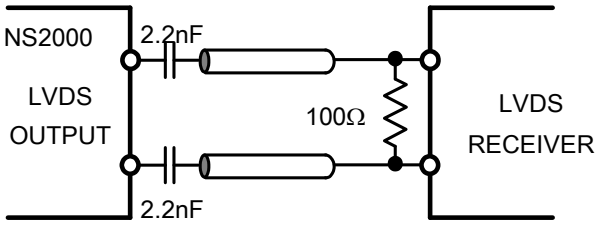
fvco=1.244GHz, fvcxo=38.88MHz,ftcxo=20MHz

OUTPUT FREQUENCY (MHz)	DUTY CYCLE (%)	RISE TIME (20%~80%)(ps)	CURRENT CONSUMPTION (mA)	DIFFERENTIAL SWING (Vp-p)
38.88	50.09	590	41.69	1.183
103.681	49.97	570	41.59	1.139
113.108	45.44	560	41.59	1.148
124.417	49.98	570	41.57	1.161
138.239	44.49	520	41.53	1.171
155.519	49.98	530	41.56	1.152
177.74	43.06	570	41.56	1.163
207.362	50.1	510	41.41	1.182
248.836	42	430	41.34	1.095
311.054	50.14	500	41.32	1.049
414.736	35.64	370	41.53	0.86
622.115	51.05	270	41.56	0.778

LVDS Suggested Termination



DC-Coupled LVDS Termination



AC-Coupled LVDS Termination

LVDS Current Consumption

fvco=1.244GHz, fvcxo=38.88MHz,ftcxo=20MHz

OUTPUT FREQUENCY (MHz)	DUTY CYCLE (%)	RISE TIME (20%~80%)(ps)	CURRENT CONSUMPTION (mA)	DIFFERENTIAL SWING (Vp-p)
38.8815	49.97	700	18.18	0.593
103.68	50.18	620	18.26	0.586
113.107	50.46	600	18.26	0.593
124.414	50.21	610	18.26	0.606
138.241	50.52	580	18.26	0.61
155.52	50.26	600	18.26	0.6
177.737	50.81	610	18.26	0.598
207.363	50.52	600	18.25	0.623
248.832	50.8	450	18.25	0.575
311.05	50.62	580	18.26	0.547
414.733	49.57	250	18.27	0.431
622.108	50.9	220	18.24	0.378

5 TAPE AND REEL SPECIFICATIONS

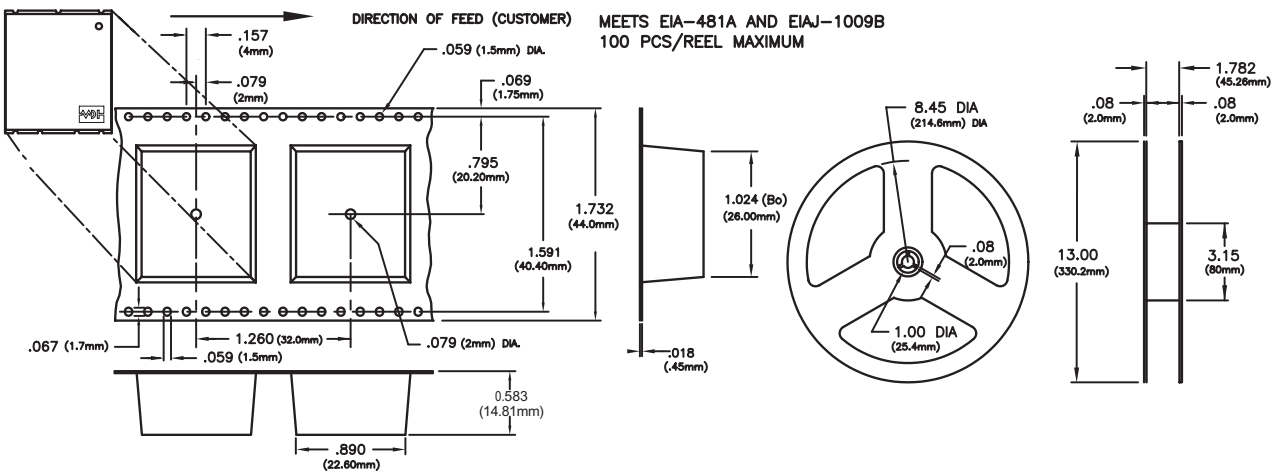


Figure 4 Tape and Reel

6 SOLDER PROFILE

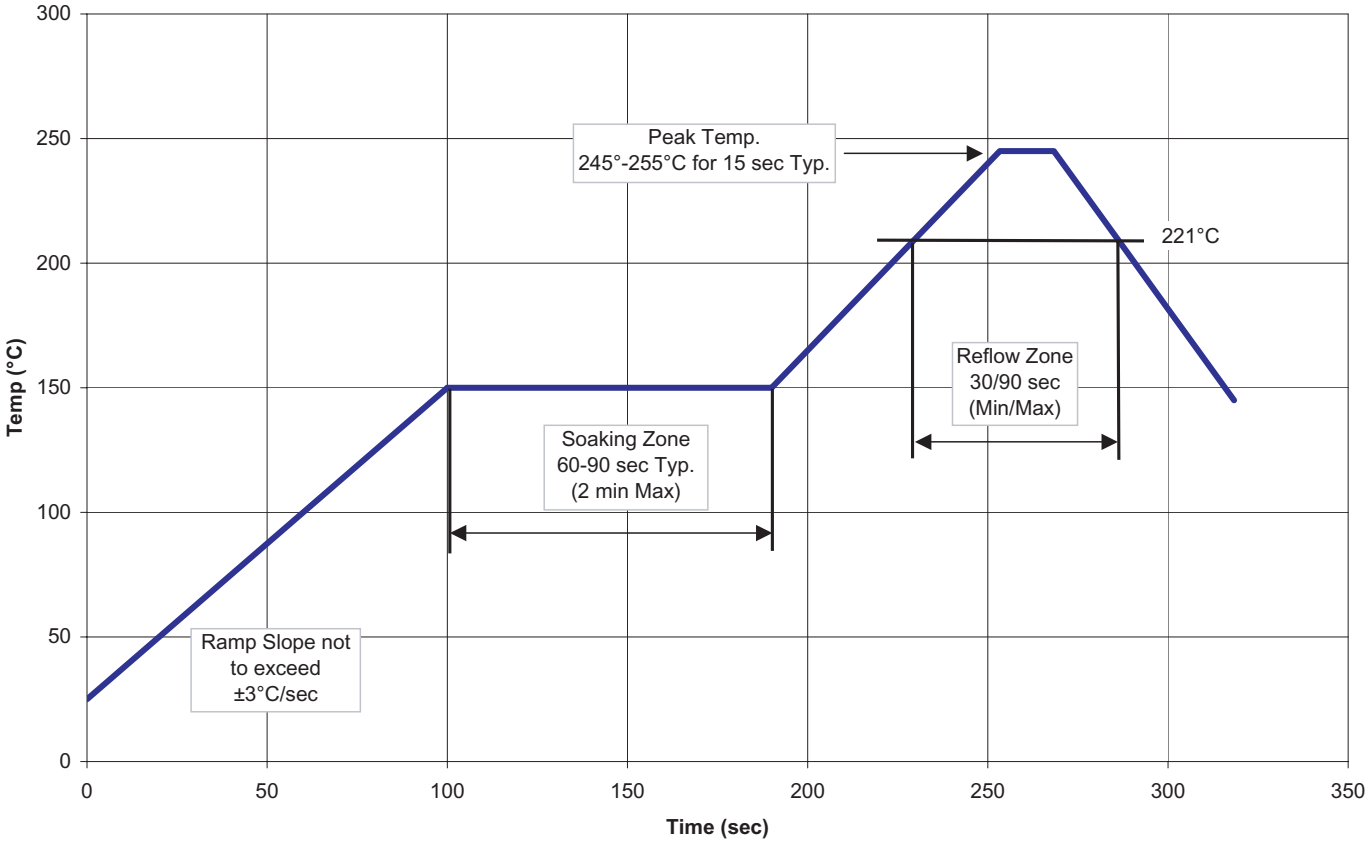


Figure 5 Solder Profile

EH320-TFC-CC-OPL
Time to Frequency Converter Module

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Ordering Information:

EH320-TFC-CC-OPL

- EH320-TFC: BASE MODEL
- CC: MCLK SUFFIX
- OPL: CUSTOM CONFIGURATION SUFFIX

MCLK Suffix	Thermal Stability	Comments
-CC	±0.5ppb; -40 to 85°C	Compensated OCXO

Custom Configuration:	-OPL
VCXO Frequency:	10.0 MHz
OUT1:	10.0 MHz LVCMOS
OUT2:	10.0 MHz Sinewave
OUT3:	10.0 MHz LVCMOS
OUT4P:	N/C
OUT4N:	N/C
OUT5:	N/C

** Any unused outputs can be turned off*

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Revision History

Revision	Date	Note
00	09/30/20	New Release